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DIGITAL AVIONICS CASSETTE TRANSFER SYSTEM AND A PROGRAM LOADER FOR IBM SYSTEM/4Pi CP-2

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This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER

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SALTY NET Program Manager
Deputy for Control
and Communications Systems

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DATA RECOVERY
ECHO CHECKING
HIGH-SPEED LOADING OF COMPUTERS
LOADING AND VERIFICATION OF 4PI CP-2
LOADING OF CP-2 WITHOUT SOFTWARE AID

(over)

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

A portable cassette transport unit, the Digital Avionics Cassette Transfer System, and a portable direct-memory-access interface, the AGE Interface, have been developed to enable field loading and verification of the System/4Pi CP-2 memory. The Digital Avionics Cassette Transfer System (DACTS) is a user programmable

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19. Key Words (Continued)

MULTIBLOCK TILES
REDUNDANT RECORDING WITH PARITY
SIMPLE INPUT/OUTPUT INTERFACE
TWELVE-OR SIXTEEN-BIT WORDS
USER PROGRAMMABLE DEVICE
VARIABLE LENGTH BLOCKS

20. Abstract (Continued)

information storage device with a general purpose parallel interface that can write or read information on a magnetic tape cassette. A cassettc can store information for at least two, 8,448 thirty-six-bit-word CP-2 memories. The AGE Interface has a general purpose parallel input, and it can load and/or verify the System/4Pi CP-2 memory without the aid of any CP-2 software. This report gives functional, hardware and operating descriptions of the DACTS and the AGE Interface with procedures to load and verify the CP-2 memory.

ACKNOWLEDGMENT

This report has been prepared by The MITRE Corporation under Project No. 6770. The contract is sponsored by the Electronic Systems Division, Air Force Systems Command, Hanscom Air Force Base, Massachusetts.

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1.0 INTRODUCTION

The use of the IBM System/4Pi CP-2 (reference 1) as the message processor in several Air Force systems requires information to be loaded into its memory. Several units are available to perform this function; however, these units cannot be made available at field sites since they are not designed to be portable. A portable cassette transport unit, Digital Avionics Cassette Transfer System (DACTS), and a portable direct-memory-access interface for the CP-2 computer, AGE Interface, have been developed to enable field loading and verification of the System/4Pi CP-2 memory. The loading and verification of the CP-2 memory, using the DACTS and the AGE Interface, require 90% less time than the existing procedure. It also reduces to half the total information required to load data into the computer's memory since the AGE Interface can load sequential memory locations of the CP-2 given the starting address followed by a block of data words. A cassette can store information for at least two, 8,448 thirty-six-bit-word CP-2 memories.

The Digital Avionics Cassette Transfer System is an intelligent peripheral device which has been designed to operate not only with the 4Pi CP-2 but with a wide range of computers. It has verification circuits to improve data reliability. It can recover an error of one bit in the twelve/sixteen bit word read with 100% certainty and an error of two bits with 50% certainty. Higher error rates with vanishingly low probability of occurrence are detectible but not recoverable. The DACTS is a user programmable device that can operate in ten different modes. The different modes of operation and the input/output interface provide the flexibility and the simplicity to enable the use of DACTS in various applications. The AGE Interface is capable of reliable high-speed loading and verification of the System/4Pi CP-2 memory. It utilizes the direct-memory-access channel, and it does not require any software to be resident in the computer's memory.

The DACTS and the AGE Interface have been in use since March 1975 and were successfully used during the 1975 SEEK BUS/AWACS European Demonstration and are currently being used on the SALTY NET Program. The DACTS and the AGE Interface are shown in Figure 1 (a). The Field Operating Unit (FOU) (reference 2), a device which is available from the International Business Machines and is capable of loading and verifying the CP-2 memory, is shown in Figure 1 (b).

This paper describes the DACTS, the AGE Interface and the procedure to load and verify the CP-2 memory using the DACTS and

Figure 1(a) Digital Avionics Cassette Transfer System (left) and AGE Interface (right)

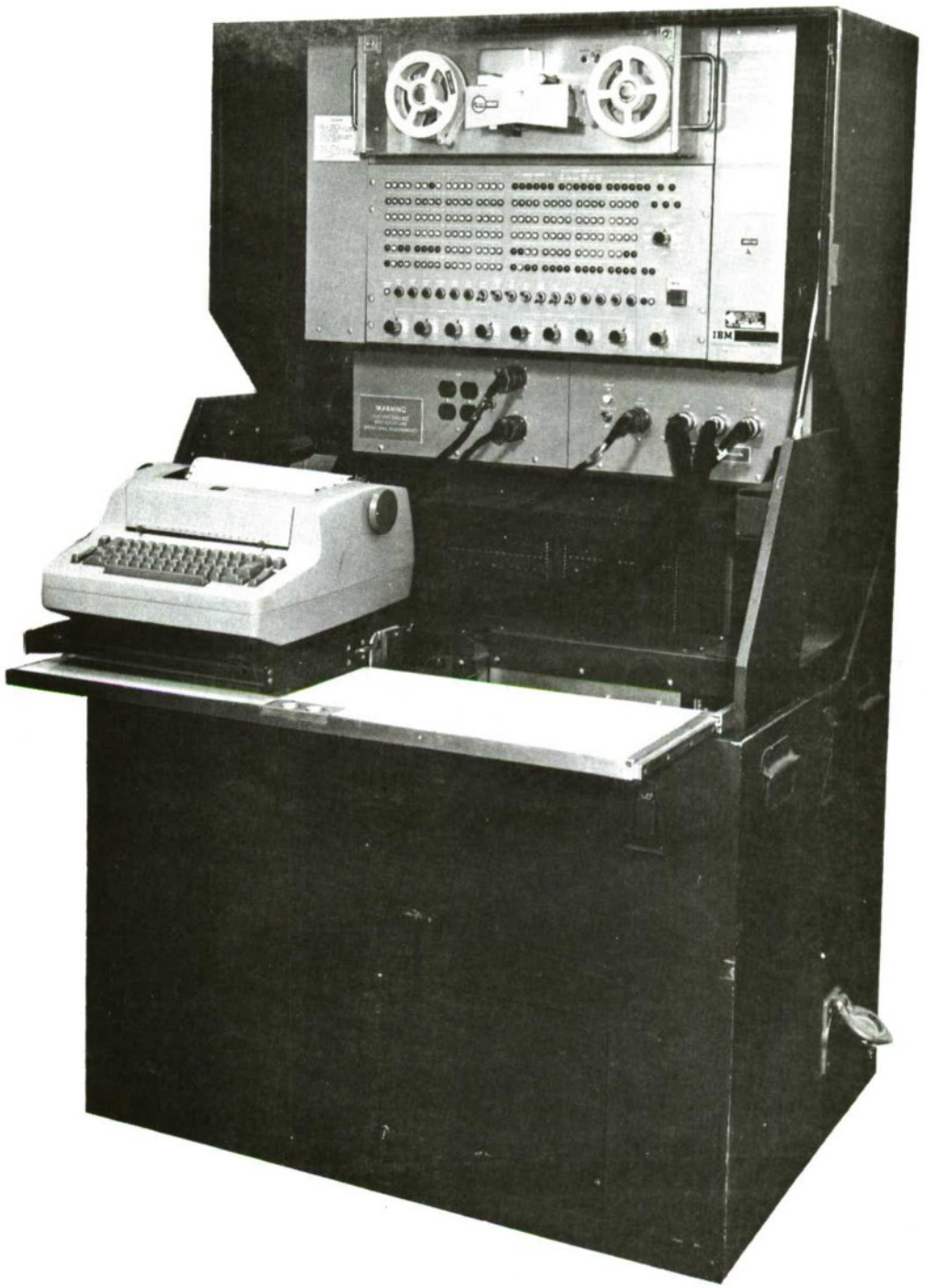


Figure 1(b) Field Operating Unit

the AGE Interface. A general description of this system is given in Section 2.0. Section 3.0 and 6.0 give detailed functional and hardware descriptions respectively, of the DACTS and the AGE Interface. Section 4.0 describes the user/status panel of the devices and also includes the procedures to record data on a cassette and to load and verify the CP-2 memory. Section 5.0 details the maintenance required and the procedure to troubleshoot the DACTS and the AGE Interface.

2.0 GENERAL DESCRIPTION

The Digital Avionics Cassette Transfer System is a user programmable peripheral device capable of storing 2.16 million bits of information on a magnetic tape cassette approved for digital use. The unit of input/output information interchange may be a twelve- or a sixteen-bit word. Every input word is recorded twice with a two-bit preamble, a two-bit suffix and a parity bit. The two words recorded for each input word are read back and compared for errors. The word read off the tape is also compared with the corresponding input word, and any errors detected are indicated on a user/status panel. The reading and the writing of information is done simultaneously since the transport (reference 3) has separate read and write heads. Echo check and redundant recording with appropriate parity improves the reliability of the data words recorded and played back by the DACTS. The information on a cassette is structured in the form of words, blocks and files. A block is composed of one or more words, and one or more blocks constitute a file on a cassette. This format enables very efficient use of the storage available on a cassette since different files can be read or recorded separately.

The DACTS is designed to be a modular unit, and its functional block diagram is shown in Figure 2. The Input Interface receives data in the form of twelve/sixteen bit words from an external device, and the received data are recorded on a magnetic tape by the Write Circuit in the Write or the Read After Write mode. Every word recorded is stored in a first-in-first-out buffer (FIFO) in the Write-Verify Circuit. The Read Circuit reads the data recorded on the magnetic tape and also detects and recovers errors in the data read. The Write-Verify Circuit compares the word read with the current output word of the FIFO to detect write data errors in the Write or the Read After Write mode. The Search Circuit performs the function of finding the file whose file name is set up on the user/status panel. The Output Interface transmits twelve/sixteen bit words read off the magnetic tape to an external device. The Next Load Point Circuit determines the end of all previously recorded information on the magnetic tape (i.e., the position on the magnetic tape where new data may be recorded) in the Write or the Read After Write mode. The DACTS has a user/status panel which is used to set up user inputs and to display the state of the unit in any mode of operation. Data errors and transport malfunction indicators are also included on the user/status panel. The Master Control Circuit controls the functioning of each module and the flow of data within the DACTS. Any module can operate in parallel with any other module to perform different functions. The DACTS

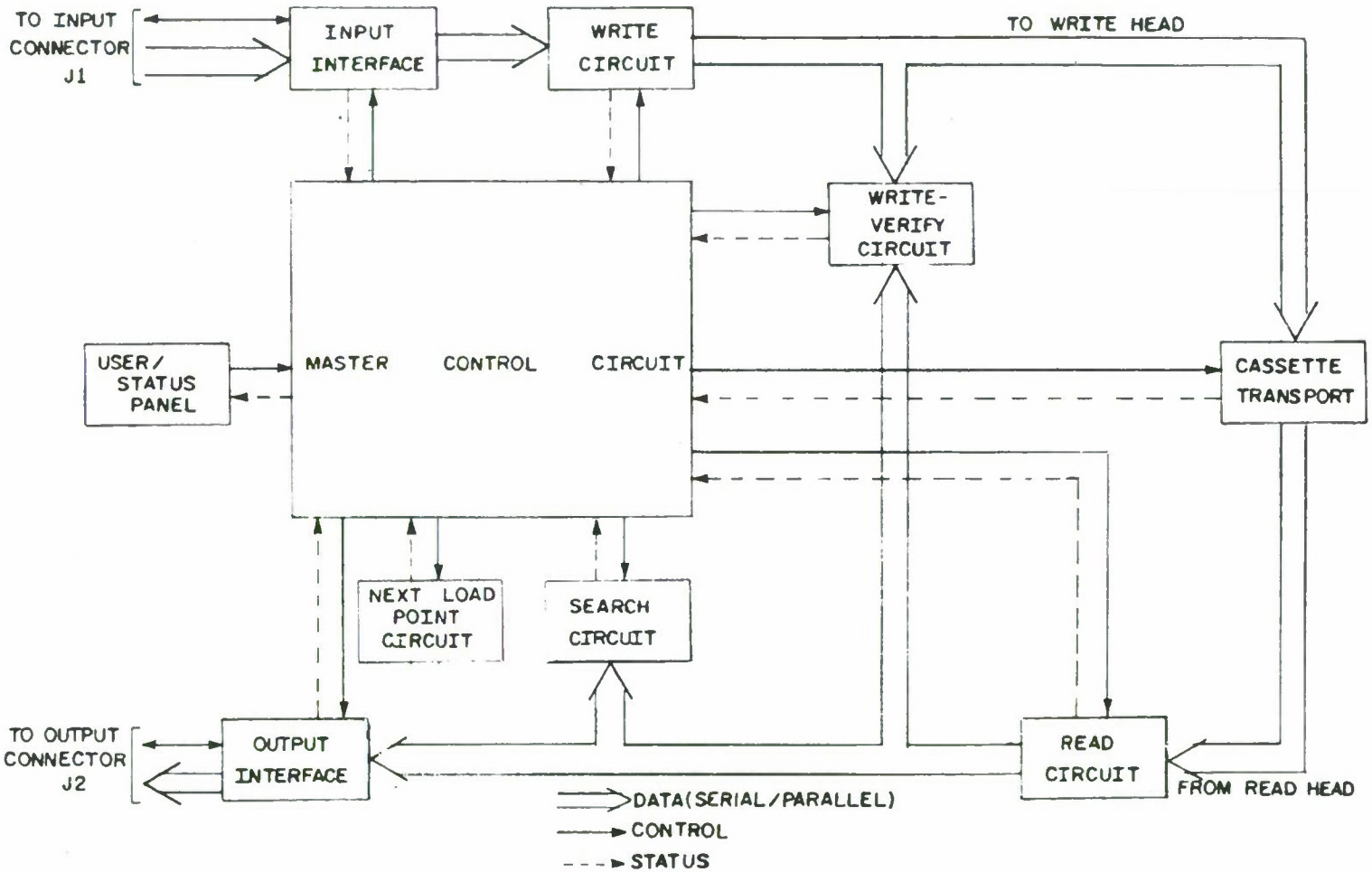


Figure 2 Functional Block Diagram of DACTS

employs a reel-to-reel transport with a read and a write head, and it uses a clock track for precise speed control. Information is recorded on the magnetic tape in the Bi-Phase-Level format to provide self-clocked data.

The AGE Interface is a portable unit capable of loading and verifying the System/4Pi CP-2 memory at a maximum rate of 250,000 words per second. It utilizes the direct-memory-access channel of the CP-2 computer, and it does not require any software to be executed to perform its functions. It extracts the address and the data words from the information received from an external device and loads the data into the appropriate System/4Pi CP-2 memory location. Every word loaded is read back and verified, and address or data errors detected are indicated on a user/status panel. The information to load the System/4Pi CP-2 memory may be in the form of an address followed by a data word to be stored at the addressed location or a starting address followed by a block of words to be loaded in consecutive storage locations. The total information required to load data into the computer's memory is considerably less when it is received in the latter form.

The functional block diagram of the AGE Interface is shown in Figure 3. It consists of three functional modules and a user/status panel. The Input Interface receives twelve/sixteen bit words from an external device, formats it into an address or a data word and sends it to the Computer Interface. The Computer Interface controls the flow of information between the AGE Interface and the System/4Pi CP-2, and it is capable of data transfer in either direction. The operation of the AGE Interface and the flow of data are controlled by the Master Control. The AGE Interface has a user/status panel to set up user inputs and to display the state of the unit in any mode of operation. The AGE Interface is designed in such a way that minimum modifications would be required to add (or substitute for Input Interface) an Output Interface to transmit the content of the System/4Pi CP-2 memory to an external device. The functional block diagrams of modified AGE Interfaces are shown in Figures 4 and 5.

The procedure to load and verify the System/4Pi CP-2 memory using the DACTS and the AGE Interface consists of three different steps. The source program is generated and cross-assembled by the Time Sharing System at the SEEK BUS Evaluation Facility. The block diagram of the Time Sharing System which stores the assembled software on a magnetic tape is shown in Figure 6. The assembled data stored on the magnetic tape are processed and formatted into a form acceptable to the DACTS by the Cassette Generator Program (reference 4) and recorded on a magnetic tape cassette, using a

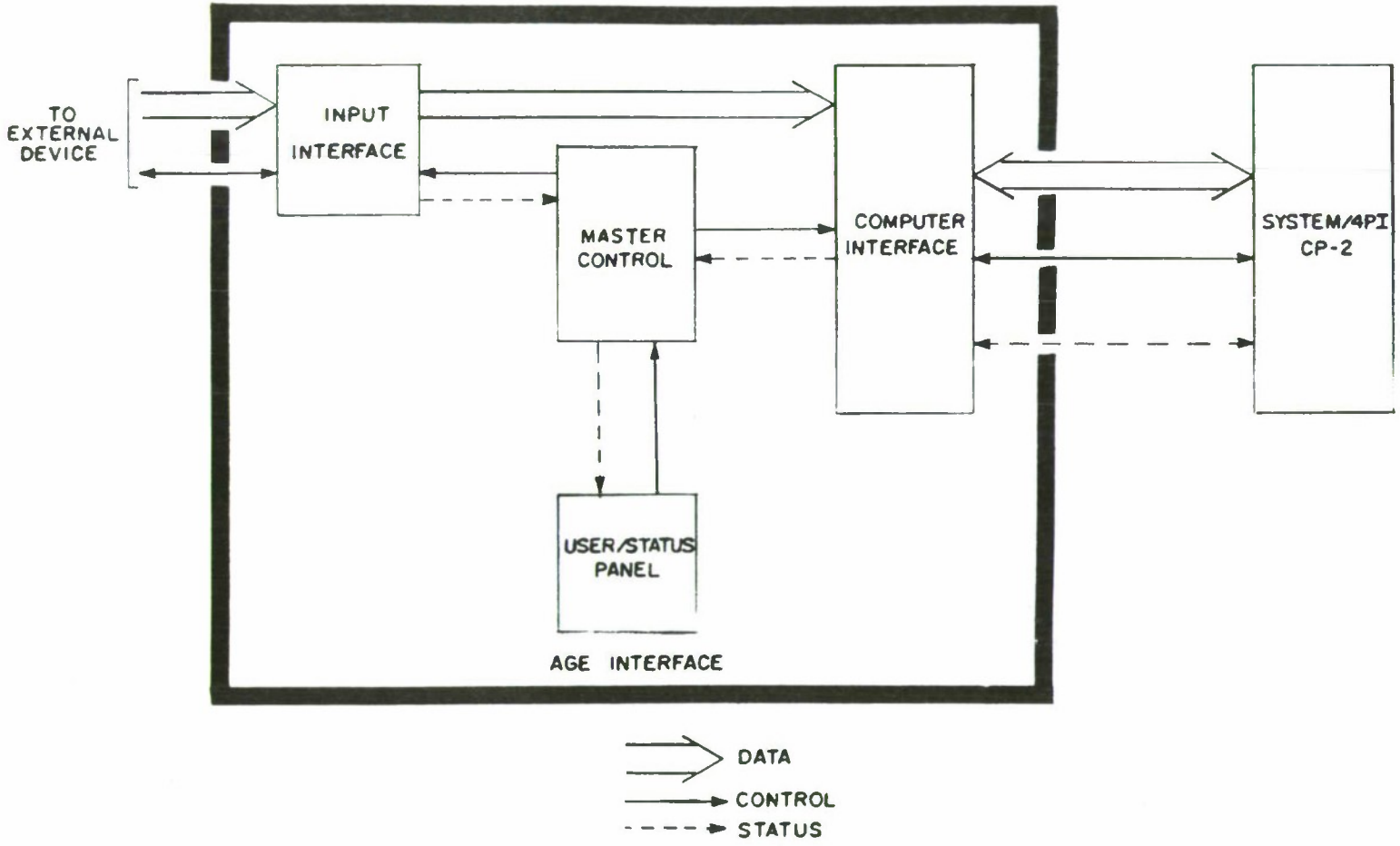


Figure 3 Functional Block Diagram of AGE Interface

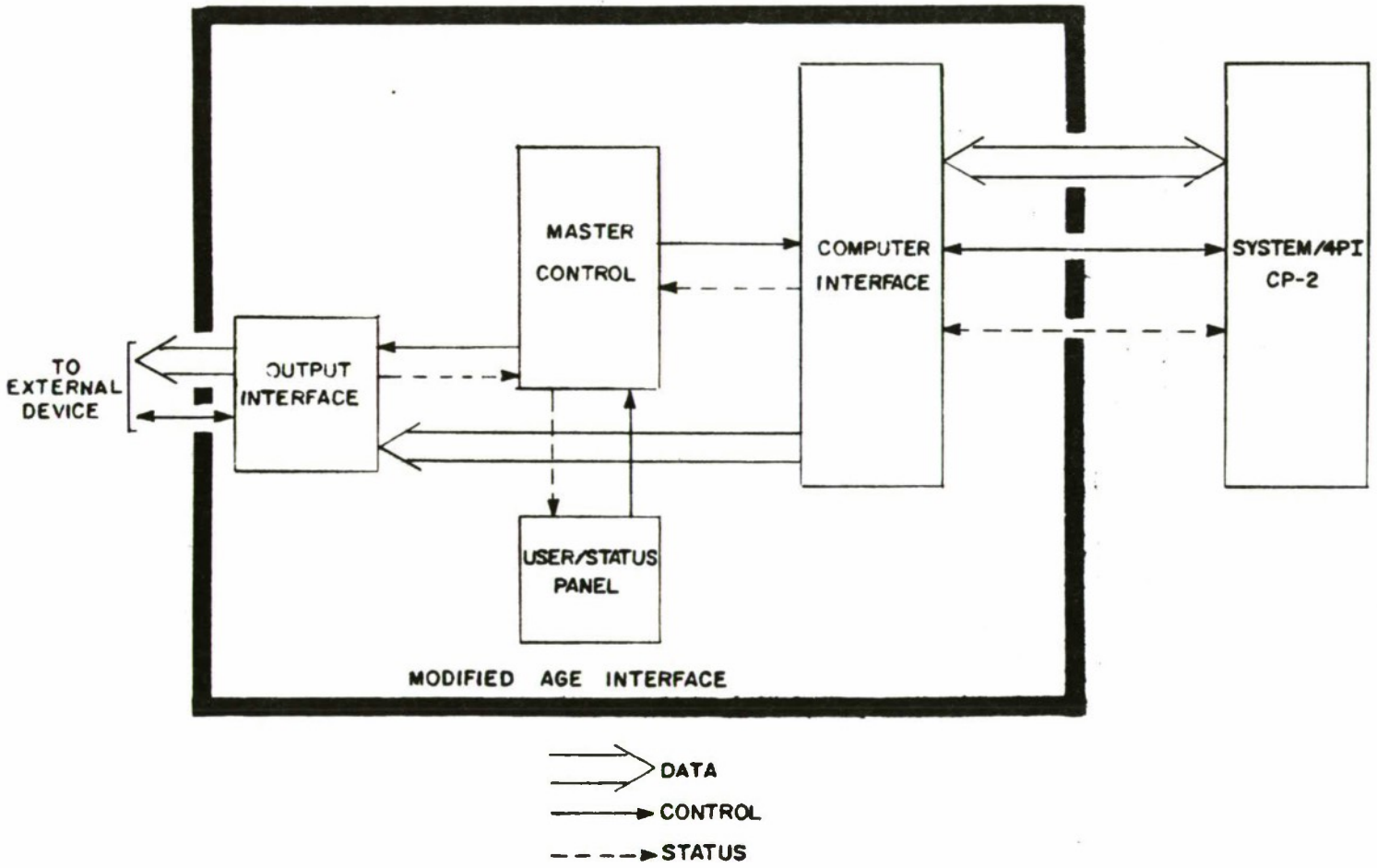


Figure 4 Functional Block Diagram of AGE Interface (Output Only)

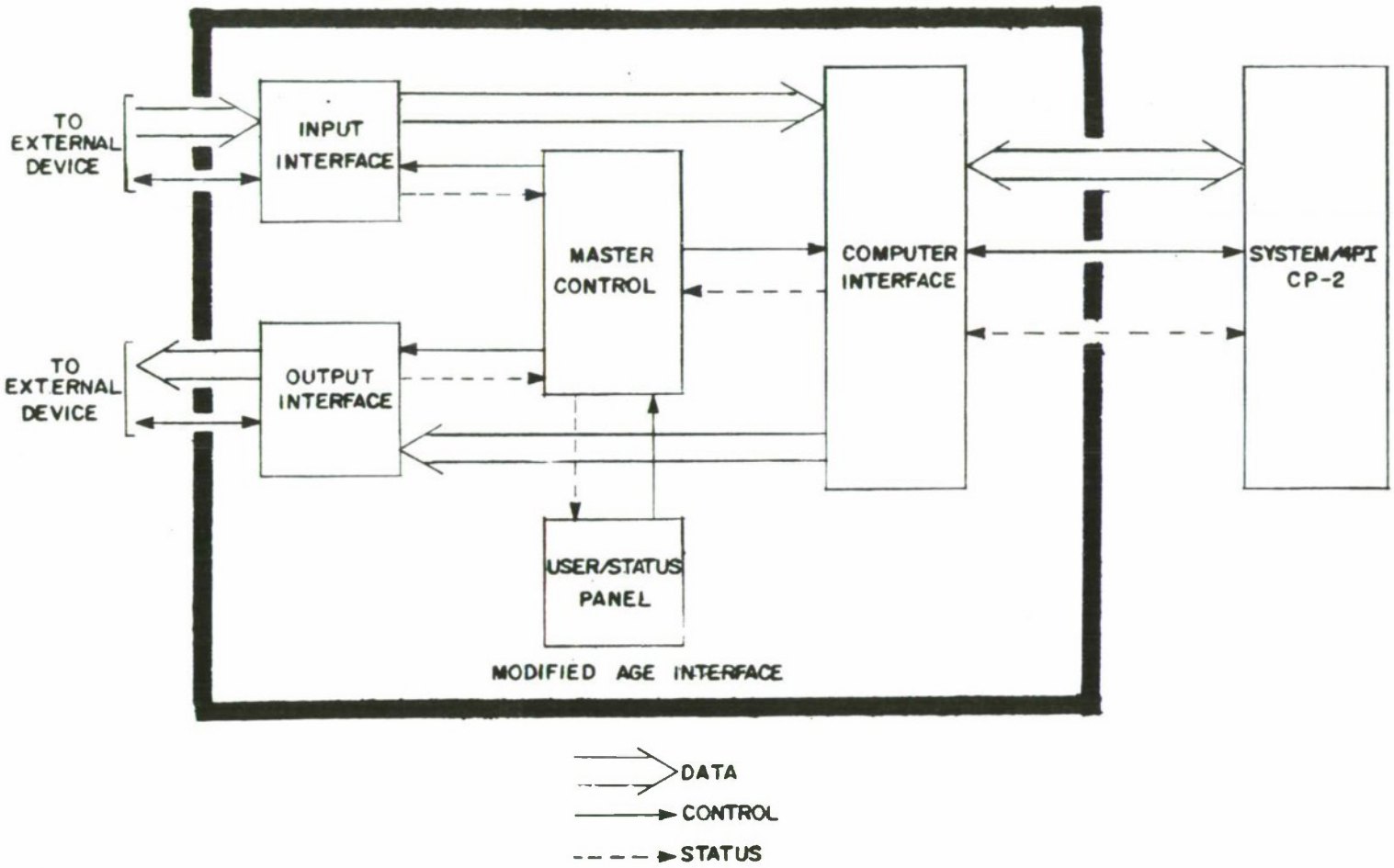
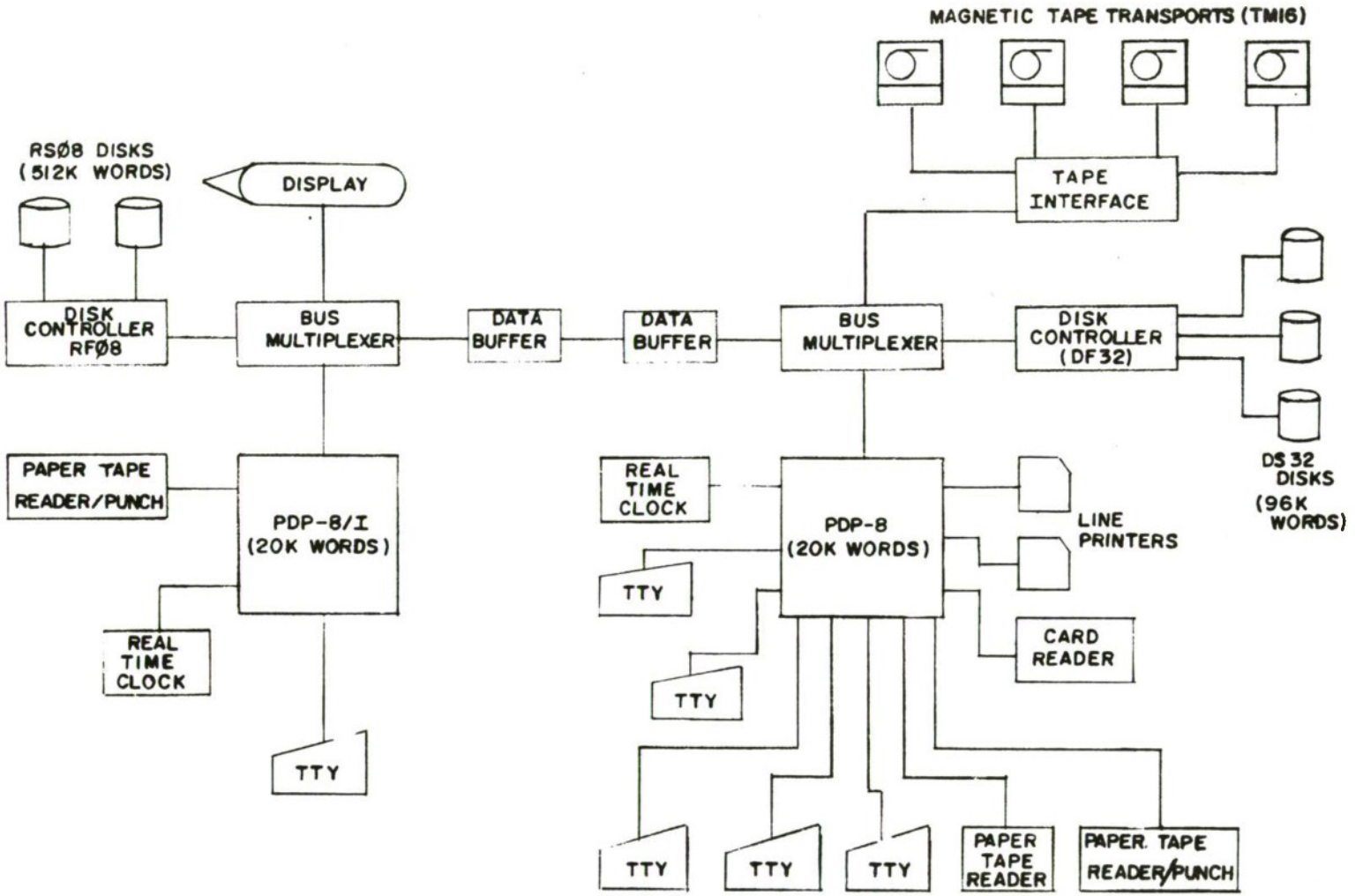


Figure 5 Functional Block Diagram of AGE Interface (Input and Output)



(i) OPERATOR INPUTS SYSTEM/4 PI CP2 SOFTWARE THROUGH A TTY.
(ii) ASSEMBLED SOFTWARE IS STORED ON A MAGNETIC TAPE.

Figure 6 Block Diagram of the Seek Bus Time Sharing System

PDP-8 minicomputer and the DACTS. The block diagram of this system is shown in Figure 7. The information recorded on a magnetic tape cassette is played back by the DACTS and loaded into the System/4Pi CP-2 memory by the AGE Interface. The block diagram of this system is shown in Figure 8. The components of the system used to generate a cassette are shown in Figure 9, and the units used to load data into the System/4Pi CP-2 memory of a SALTY NET terminal are shown in Figure 10.

A summary of characteristics of the DACTS and the AGE Interface is given in Table I.

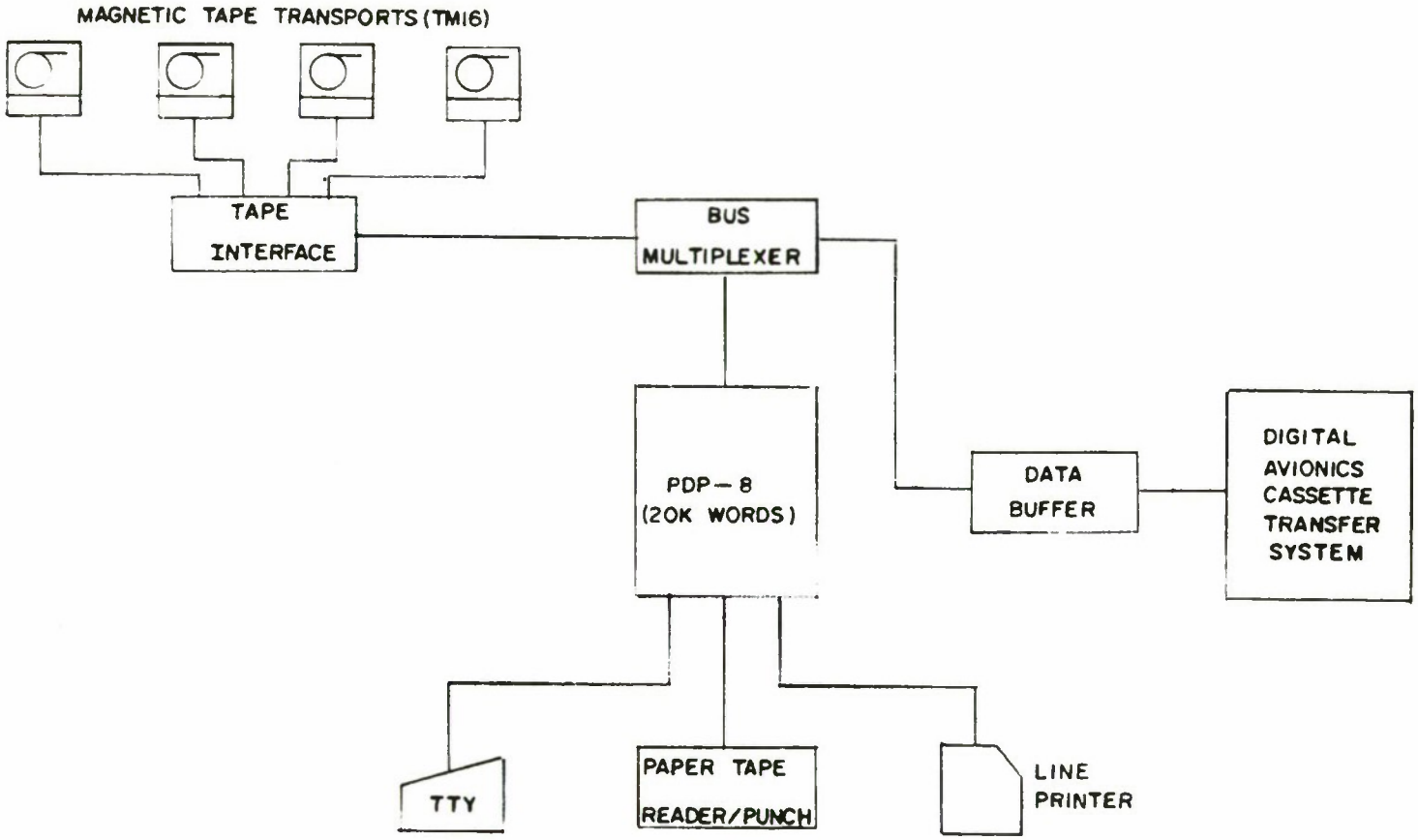


Figure 7 Block Diagram of Cassette Generator System

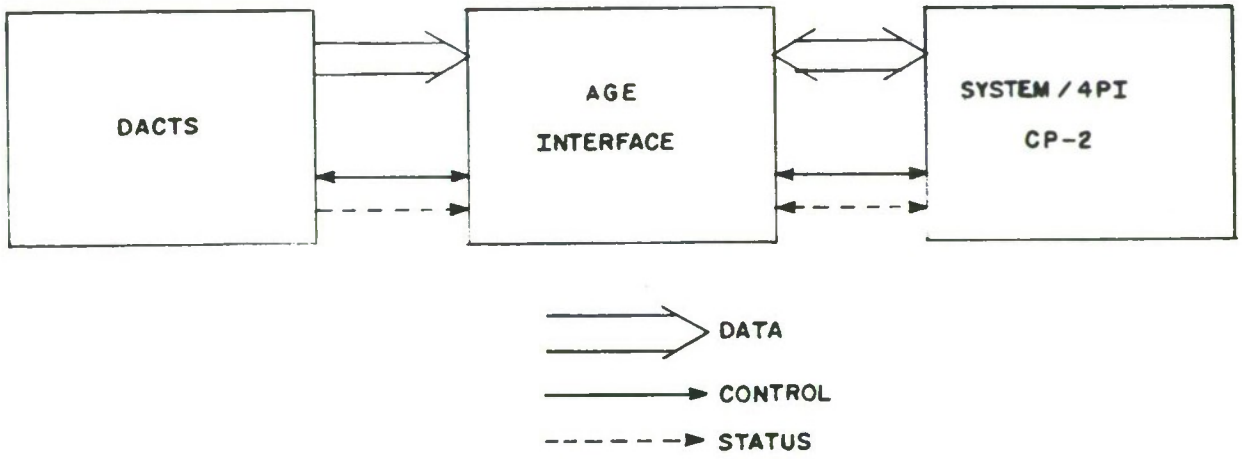


Figure 8 Block Diagram of System/4Pi CP-2 Loading and Verifying System

Figure 9 Units Used to Generate Cassettes; Rear (left to right): Paper Tape Reader, PDP-8 and Magnetic Tape Transport. Middle (left to right): DACTS Power Unit and DACTS. Front: Teletype

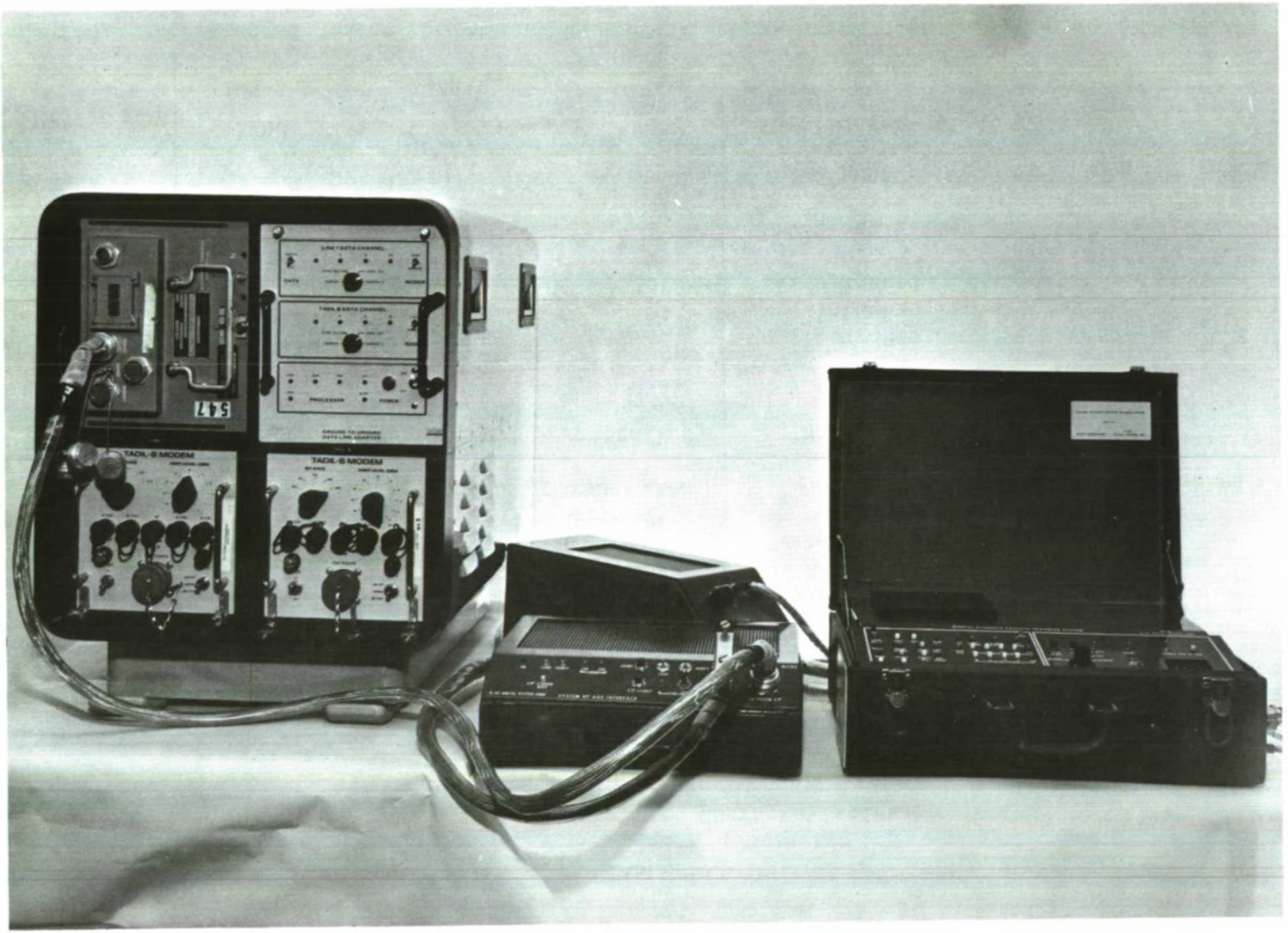


Figure 10 Units Used to Load Information into System/4Pi CP-2 Memory; Front (from left to right) Salty Net Terminal with a System/4Pi CP-2, AGE Interface and DACTS; Rear: DACTS Power Unit

TABLE I

DACTS and AGE Interface Characteristics

	DACTS	AGE INTERFACE
Type	Magnetic tape cassette unit	Loads and verifies CP-2 memory
Data Word	Twelve/sixteen bits	Twelve/sixteen bits
Input	One channel-externally controlled	One channel-externally controlled
Output	One channel-internally controlled	None
Dimension		
Width	17.75 inches	14 inches
Height	6 inches	4 inches
Depth	12.50 inches	11.75 inches
Volume	0.77 cubic feet	0.38 cubic feet
Weight	22 pounds	15.5 pounds
Power	(+5VDC, 12A); (-5V, 250 mA); (105-132 VAC, 57-63 Hz)	105-132 VAC, 57-63 Hz
Cooling	Keep air inlet/outlet unblocked	Keep two inch space on top of unit

3.0 FUNCTIONAL DESCRIPTION

Digital Avionics Cassette Transfer System is a portable input/output device which can interchange information with any unit with the same input/output specifications as that of the General Purpose Parallel Interface of the Control/Display Unit for System/4Pi CP-2. It can also communicate with a PDP-8, PDP-8/I, PDP-8/E or a PDP-15 minicomputer equipped with an appropriate data buffer. DACTS can record/playback information on/from a magnetic tape cassette.

The process of recording information on a cassette is complex and requires parallel functioning of five of the six modules (Figure 2). Extensive checking is done to ensure proper functioning of all the different modules. Every word received is recorded twice on the digital cassette with a two-bit preamble, a two-bit suffix and a parity bit. The word recorded is stored in a first-in-first-out (FIFO) buffer. The words recorded are then read back, and the two recorded words for the same input word are compared. If they are equal then one of them becomes the word read. If they are unequal then parity test is performed, and the word that satisfies the odd parity requirement becomes the word read and an error condition is indicated. The word read is then compared with the current output of the FIFO. If these two words are unequal, a write error is indicated. Thus, the input words are written, read and verified. If the Read After Write mode is selected then the word read is made available to an external device through the output connector.

The information is recorded on the cassette in the form of seventeen/twenty-one bit word for every twelve/sixteen bit input word. This is followed by an interword gap equivalent to four bit times. After the interword gap, the unit of seventeen/twenty-one bits for the same input word is duplicated. This is followed by an interword gap and then a unit of seventeen/twenty-one bits for the next input word. One or more words recorded as described above constitute a block. Blocks of words are separated by interblock gaps. The size of the block is determined by the external device from which the information is received by DACTS. One or more blocks form a file, and consecutive files are separated by an interfile gap. The start of a file is indicated by the initial start up procedure and the mode of operation of DACTS. The first word of the file received from the external device is recorded as the file name. The file name is followed by a file gap and then the information to be recorded in that file. This file gap is

required for the cassette to stop after the file searched for is found in a DACTS mode. The second most significant bit of the file name is used by the external device to inform DACTS if the unit of input will be a twelve/sixteen bit word. The ten least significant bits of the file name indicate the actual file name to be used to address that particular file. The format used by DACTS to record information on a cassette is illustrated in Figure 11.

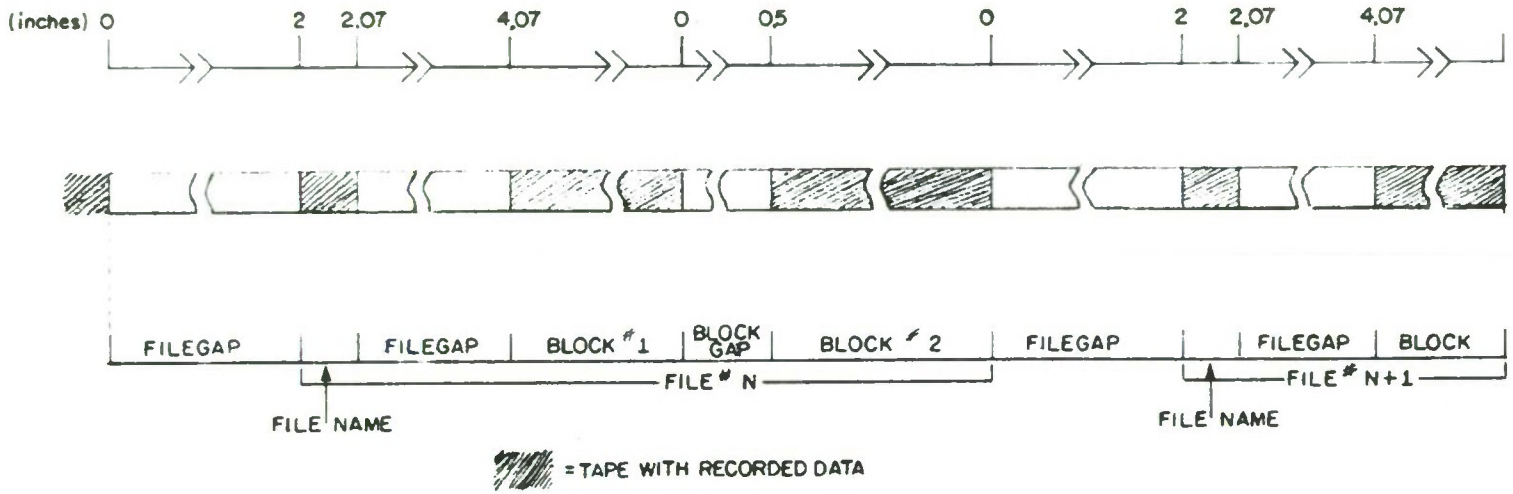
The information is recorded and played back by DACTS at a tape speed of 10 inches per second. The bit density used is 600 bits per inch. This gives a recording rate of 6000 bits per second. The digital cassette used conforms with the standards of the American National Standards Institute, European Computer Manufacturers Association, and the International Organization of Standarization. The cassette contains 300 feet of computer grade tape certified for zero dropouts and dropins. The tape has a hole between the two tracks about 20 inches from its ends for optical detection of the end/beginning of tape. It has two tracks of which track A is used for writing and reading information, and track B contains a prerecorded clock track written at 1600 flux changes per inch. This clock track is used to control the speed of the tape. The transport used has the option of multi-speed operation; the rewind speed used is 40 inches per second, and the tape is moved forward at 10 inches per second. The information is recorded on the digital cassette using the Bi-Phase-level (also called Split Phase or Manchester II + 180°) technique. In this method a "one" is represented by a flux transition toward the erase (magnetic north) direction, and a "zero" is represented by a flux transition away from the erase level in a magnetic south direction. Additional flux transitions are written at midpoints between bit flux transitions to establish proper polarity for the succeeding bits. This phase encoding scheme has the following advantages:

a. It provides higher bit density;

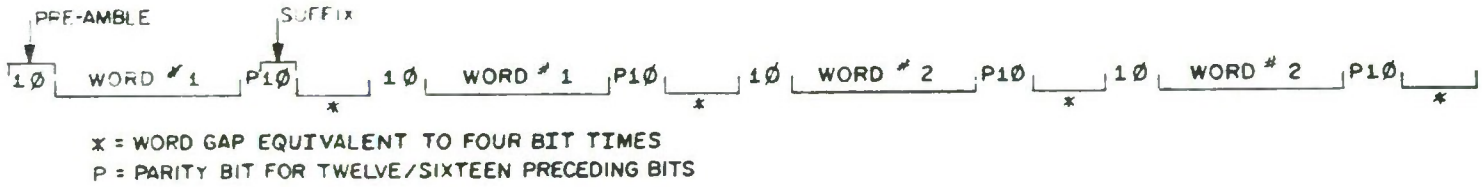
b. It provides read-after-write capability with acceptable crosstalk characteristics;

c. It ensures that a flux transition occurs in every bit cell to provide self-clocking on a single track;

d. It eliminates the problem of data recovery due to tape skew between the clock track and the data track.



(i) FILES AND BLOCKS ON A MAGNETIC TAPE CASSETTE



(ii) WORDS ON A MAGNETIC TAPE CASSETTE

Figure 11 Tape Format

Figure 12 gives the timing diagram for writing and reading of eight bits on a magnetic tape using Bi-Phase-Level recording technique. To write and read or to read, the forward motion command is enabled. For write and then read, the WRITE mode signal is enabled and the WRITE clock is generated. The frequency of this clock determines the bit density of the information recorded on the magnetic tape. When the WRITE DATA BLOCK signal is enabled, the recording of information on the tape is initiated. This signal should not be enabled until after the tape moves at the appropriate speed. This delay is about 50 milliseconds for a speed of 10 inches per second. In the WRITE mode, if WRITE DATA BLOCK is not enabled then the magnetic tape is erased. During the writing process, the current through the WRITE head changes according to the bit to be written, and this causes flux changes on the magnetic tape. When the tape passes by the read head, the data and the read clock are generated from the flux changes on the magnetic tape. The information on the tape is read by the read head when a motion command in either direction causes the tape to move at any speed. Using the technique described above, it is possible to record about 54,000/46,000 12/16 bit words on a 300 feet magnetic tape cassette.

Digital Avionics Cassette Transfer System can be operated in five basic modes. These modes are explained below:

READ mode: In this mode the information on the cassette is read and transmitted to an external device via the output connector. In a normal operation, the FILE option is enabled and the File Name of the file to be read set up as an input. The unit goes to SEARCH mode and searches for the file with the input file name. When found, it reads the file and stops at the end of that file. If the file is not found on the cassette then an indication to that effect is made. If the FILE option is not used then the information on the whole cassette is read. READ mode can also be used with the VERIFY and FILE options enabled. In this mode, the unit searches for the file, reads it when found and at the end of the file, rewinds (see explanation below) to the Initial Load Point. Then it goes into VERIFY mode, searches for the file and reads it when found. The unit stops at the end of the verification of the file. READ mode with VERIFY and FILE options enabled can be used to send information stored in a file on the cassette to an external device and then verify it by reading it the second time.

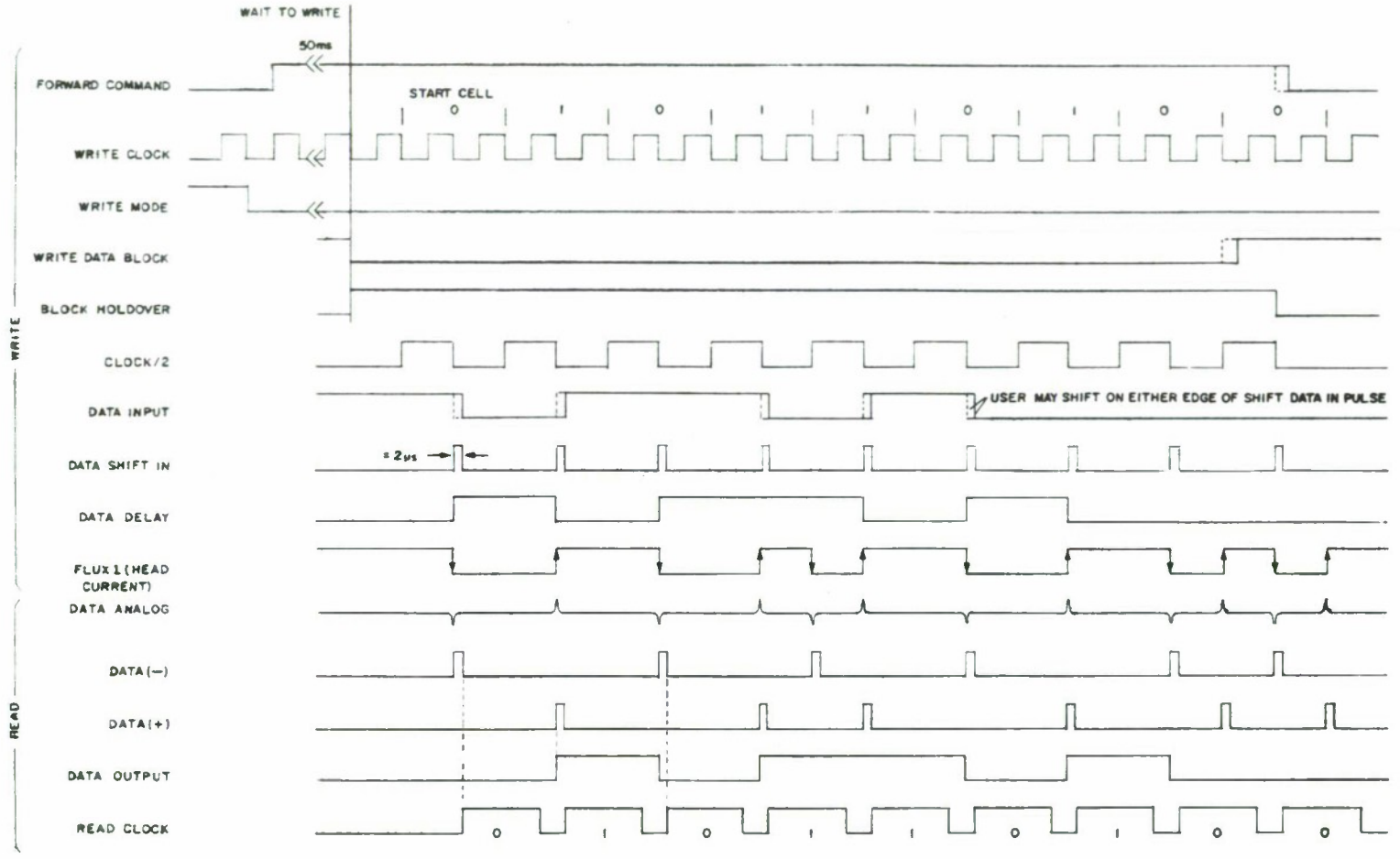


Figure 12 BI-Phase-Level Timing Diagram

REWIND mode: Information is not recorded on the cassette starting from physical beginning of tape. The recording starts about 3-3.5 inches after the optical beginning of tape (moving in the forward direction). In this mode, the transport rewinds the tape to the physical beginning of tape at 40 inches per second and then the tape is moved forward at 10 inches per second. The forward motion command is terminated about an inch after the optical end/beginning of tape is encountered and the tape motion terminates after the tape has traversed another 0.5 inches. This point where the tape stops in this mode is called the Initial Load Point (ILP). The tape also rewinds to the ILP when the system is reset using the SYSTEM RESET pushbutton. Figure 13 shows ILP on a tape.

READ AFTER WRITE mode: In this mode, information received from an external device through the input connector is written on the cassette by the write circuit. This information is then read by the read circuit, verified and made available to an external device via the output connector. This mode can be used if the external device recording the information is capable of verifying it to increase the reliability of the information stored on the cassette. This mode is recommended for use in generating cassettes for loading System/4Pi CP-2 memory.

SEARCH mode: In this mode, DACTS reads the file names of files recorded on the cassette and compares it with the file name supplied by the operator using the File Name thumbwheel switch on the user panel. When the file is found, it stops in the file gap following that File Name. If the file is not found on the cassette then an indicator to that effect is made on the User/Status Panel. This mode may be used to verify the existence of files supposed to have been recorded on the cassette.

WRITE mode: In this mode, the information received from an external device, via the input connector, is written on the cassette by the write circuit and also stored in a first-in-first-out (FIFO) buffer. This information is then read by the read circuit and every word compared with the corresponding word stored in the FIFO. Errors on echo check are indicated on the User/Status Panel. If the Next Load Point option is enabled in this mode then the system searches for that part of the cassette where all previously recorded files end and then goes to WRITE mode. If there is no information previously recorded on the cassette then the cassette will

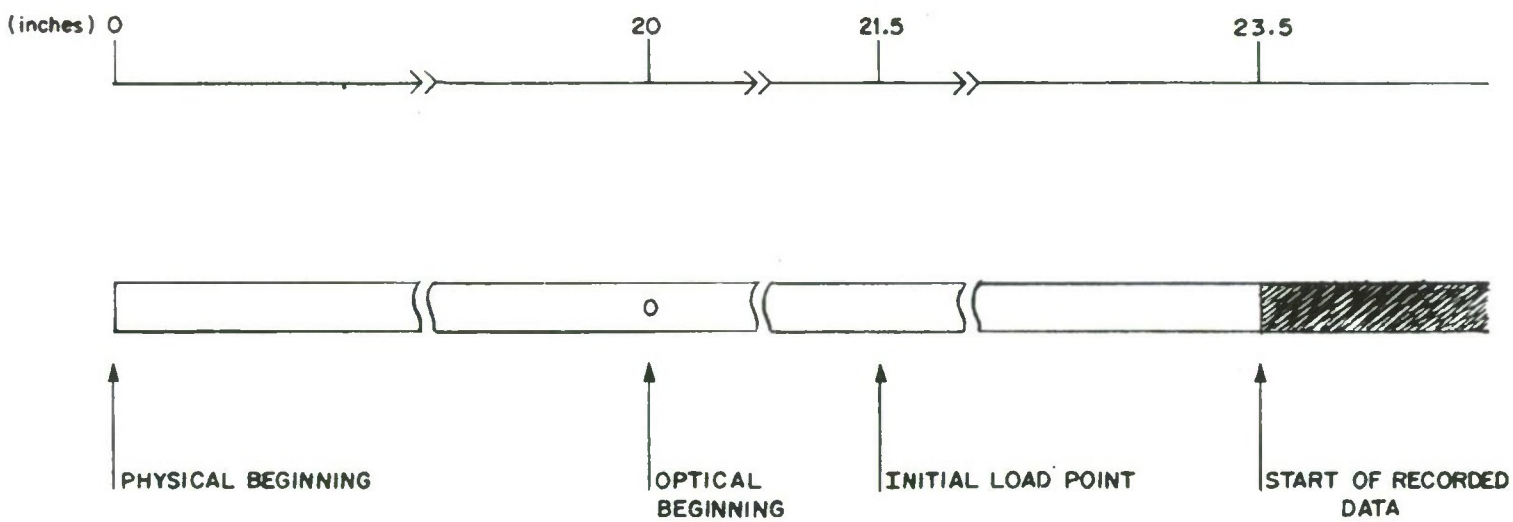


Figure 13 Initial Load Point on a Magnetic Tape Cassette

rewind and go to the Initial Load Point, and if no space is available on the cassette for recording any more information then the system will indicate that the cassette is full. If more than one file is to be recorded on a cassette then the Next Load Point option should be enabled in WRITE mode. The File Continue option used with this mode enables multi-block files. If the File Continue option is not enabled then each input block is recorded as a file with the first word used as the File Name. The File Continue option will be enabled while generating cassettes for loading System/4Pi CP-2 memory. In WRITE mode a cassette may be erased by inserting an appropriate plug into the erase socket. All cassettes on which information has to be written starting from the Initial Load Point should be erased first.

Table II summarizes the modes of DACTS. DACTS can be used in several different ways depending on a particular application. For the purpose of loading System/4Pi CP-2 memory, cassettes may be generated, using the WRITE mode with Next Load Point and File Continue options enabled. Next Load Point option may not be used for recording only one file on a cassette. This is not recommended as it results in inefficient utilization of the available storage on a magnetic tape cassette. The information for loading System/4Pi CP-2 memory may be read by using DACTS in READ mode with FILE option enabled and File Name for the file to be read supplied by the user via the file name thumbwheel switch on the User/Status Panel.

Digital Avionics Cassette Transfer System can interchange information with any system that has the same input/output specifications as that of the General Purpose Parallel Interface of a Control Display Unit of System/4Pi CP-2. The I/O transfers between DACTS and an external unit employs three control signals, twelve/sixteen data lines for each transfer direction and a status signal on the output connector. These are shown in Figure 14. The control and status signals for each transfer direction are explained below. Figure 15 gives the timing diagram for the control signals.

IDLE - It is a differential TTL signal that transitions from high to low state to indicate start of a block. In Read, and Write or Read After Write mode with File Continue option disabled, it also indicates the start of a file/message. In Write or Read After Write mode with File Continue option enabled, the first high to low state transition indicates the start of a file/message and all subsequent transitions from high to low state indicate the start of a block. It

TABLE II

Summary of DACTS Modes

MODE	OPTIONS	FUNCTION
READ	-	Reads the whole cassette
READ	FILE	Reads the file named
READ	VERIFY	Reads the whole cassette twice
READ	FILE + VERIFY	Reads the named file twice
REWIND	-	Positions tape to Initial Load Point
READ AFTER WRITE*	-	Write and read uni-block files
READ AFTER WRITE*	FILE CONTINUE	Write and read multi-block files
SEARCH	-	Find the file named
WRITE*	-	Write uni-block files
WRITE*	FILE CONTINUE	Write multi-block files

* Next LOAD POINT must be enabled

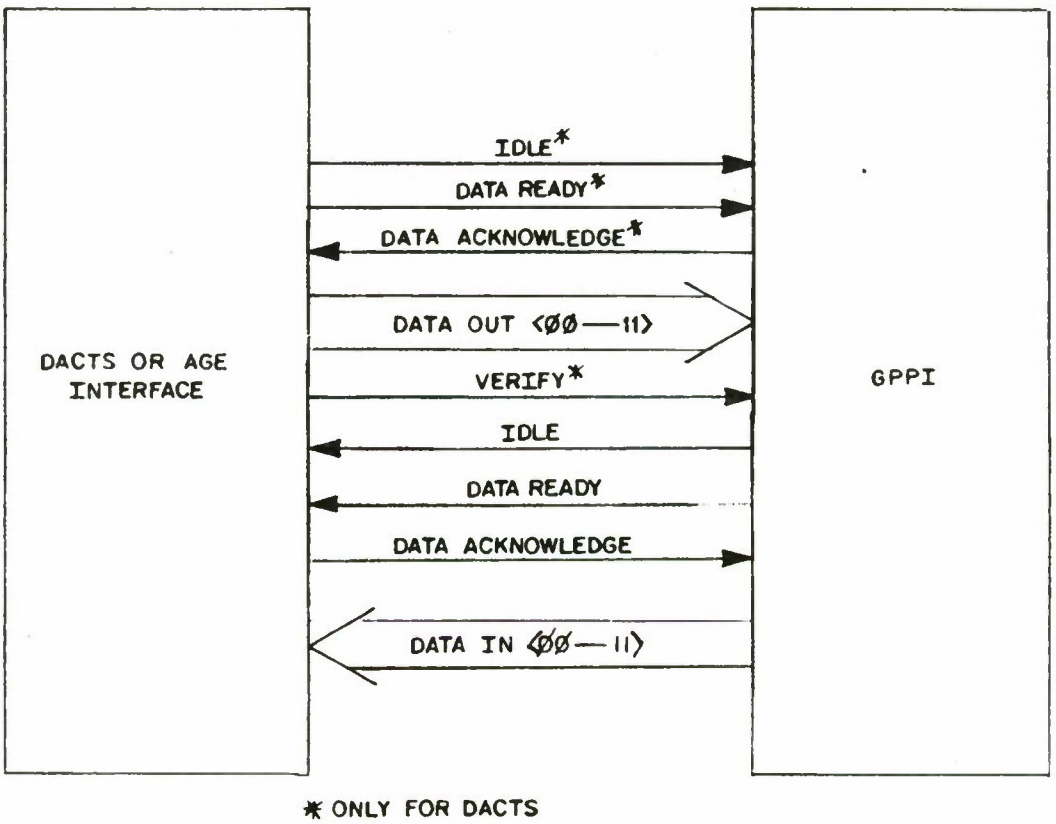


Figure 14 Signals Between a DACTS or AGE Interface and a General Purpose Parallel Interface

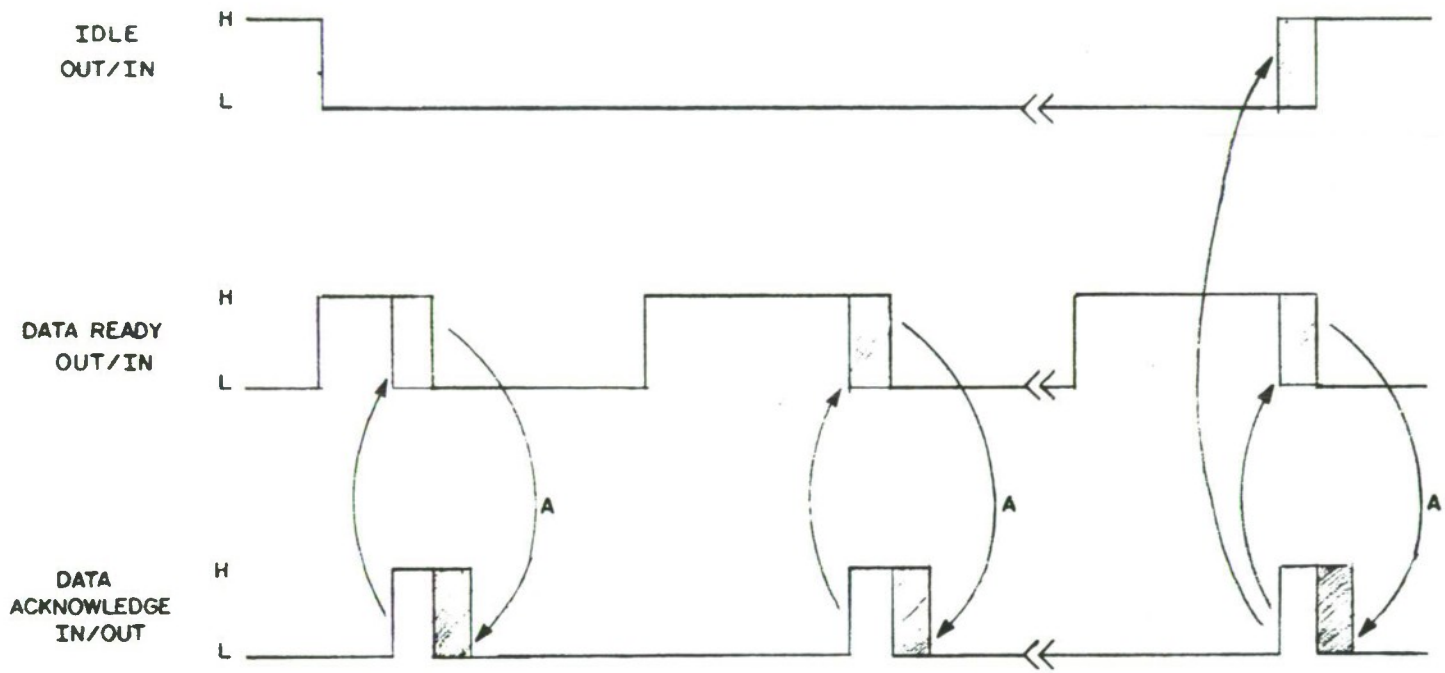


Figure 15 DACTS Input/Output or AGE Interface Input Control Signals

remains in the low state during the block/file and transitions from low to high state at the termination of the block/file (after the low to high state transition of the DATA ACKNOWLEDGE for the last word of the block/file). This signal is also referred to as BUSY, in which case it transitions from low to high state to indicate the start of a block/file, remains in the high state for the duration of the block/file and transitions from high to low state at the end of the block/file.

DATA READY - It is a differential TTL signal. When in the high state it indicates the presence of stable data on the DATA lines, and it transitions from high to low state when the DATA ACKNOWLEDGE signal transitions from low to high state.

DATA ACKNOWLEDGE - It is a differential TTL signal. A positive pulse of minimum width one microsecond or a transition from low to high state on this line indicates that the word on the DATA lines has been accepted. It transitions (in the latter case) from high to low state after the DATA READY goes to low state.

VERIFY MODE - It is a TTL signal available on the output connector. When in the low state, it indicates that DACTS is operating in the VERIFY portion of READ mode with VERIFY option enabled.

DACTS can be interconnected with other systems via two connectors. One is used for input and the other for output. Tables III and IV give the signal names associated with the input and the output connectors, respectively.

The alternate procedure to load System/4Pi CP-2 memory utilizes a DEC PDP-8 minicomputer to generate cassettes on DACTS. The information is generated for each partition of the System/4Pi CP-2 software and stored on the cassette, using the minicomputer's direct-access memory channel, in the form of blocks of maximum size of 4096 twelve bit words. If any partition of System/4Pi CP-2 software requires more than 4096 twelve bit words then it is stored on the cassette in the multi-block form. Several partitions can be stored on the cassette as part of the same file. The information stored on the cassette is read by DACTS and sent to System/4Pi CP-2 AGE Interface. The AGE Interface stores it into System/4Pi CP-2 memory using direct-memory access.

TABLE III

DACTS - Input

Signal Name	Winchester MRE 42 Pin Number	Description
IDLE H	J1 - DD	Shielded Twisted Pair
IDLE L	CC	
SHIELD	-	
DATA READY H	HH	Shielded Twisted Pair
DATA READY L	FF	
SHIELD	-	
DATA ACKNOWLEDGE H	LL	Shielded Twisted Pair
DATA ACKNOWLEDGE L	KK	
SHIELD	EE	
DATA BIT ØØ	A	Single Wires
Ø1	B	
Ø2	C	
Ø3	D	
Ø4	E	
Ø5	F	
Ø6	H	
Ø7	J	
Ø8	K	
Ø9	L	
1Ø	M	
11	N	
12	P	
13	R	
14	S	
15	T	
DATA GROUND	U	
SHIELD	V	Overall Shield

TABLE IV

DACTS - Output

Signal Name	Winchester MRE 42 Pin Number	Description
IDLE H	J2 - DD	Shielded Twisted Pair
IDLE L	CC	
SHIELD	MM	
DATA READY H	HH	Shielded Twisted Pair
DATA READY L	FF	
SHIELD	JJ	
DATA ACKNOWLEDGE H	LL	Shielded Twisted Pair
DATA ACKNOWLEDGE L	KK	
SHIELD	-	
VERIFY MODE	AA	Twisted Pair
GROUND	BB	
DATA BIT ØØ	A	Single Wires
Ø1	B	
Ø2	C	
Ø3	D	
Ø4	E	
Ø5	F	
Ø6	H	
Ø7	J	
Ø8	K	
Ø9	L	
1Ø	M	
11	N	
12	P	
13	R	
14	S	
15	T	
DATA GROUND	U	
SHIELD	V	Overall Shield

AGE Interface can be used to store information into System/4Pi CP-2 memory and verify each word after it is stored in LOAD mode or to verify information in System/4Pi CP-2 memory in VERIFY mode. It can receive information in the form of twelve/sixteen bit words. The input words are converted into words of eighteen bits where the two most significant bits are used to determine the type (data/address) of the sixteen bit word. If the reformatted input word is an address then it is loaded into Current Address Register (CAR). The value of CAR gives the address of the System/4Pi CP-2 memory location where the next data word will be stored. If the reformatted input word is a data word and the AGE Interface is in Verify mode or after the word is stored in Load mode, the Storage Address Register and the Storage Data Register of System/4Pi CP-2 are read and compared with the content of CAR and the data word, respectively. Errors, if any, are indicated on the user panel. At the end of the verification process CAR is incremented by one, and the next reformatted input word is accepted. To load information into System/4Pi CP-2 memory it is necessary to provide an address and the word to be stored at that address. An address may precede every data word, but this requires half the information to be address words. To reduce the amount of information required to store data into System/4Pi CP-2 memory, CAR is used so that only the starting address is required to store data into blocks of sequential storage locations. This technique considerably reduces the information required to load software into System/4Pi CP-2 memory.

AGE Interface may be operated in three different modes. These are explained below:

LOAD mode: In this mode the information received is reformatted and data loaded into appropriate locations of System/4Pi CP-2 memory. After each data word is stored the Storage Data Register and the Storage Address Register are read and compared with CAR and the data word, respectively. Errors, if any, are indicated on the User/Status Panel.

VERIFY mode: In this mode the information stored in the System/4Pi CP-2 memory is compared with the information received by the AGE Interface. Errors, if any, are indicated on the User/Status Panel.

LOAD-VERIFY mode: In this mode of operation the AGE Interface goes to LOAD mode when the file is received for the first time, and when the same file is received a second time the AGE Interface goes to VERIFY mode. In each mode it performs the functions explained above.

Execution of a program in System/4Pi CP-2 memory can be initiated by resetting the computer via 4π SYSRST pushbutton on the User/Status Panel of AGE Interface. To load information into System/4Pi CP-2 memory the AGE Interface may be used in LOAD mode. VERIFY mode may be used to determine if the System/4Pi CP-2 memory has the appropriate information stored in its memory. Both these modes require DACTS to be operated in READ mode with the FILE option enabled. The LOAD-VERIFY mode requires DACTS to be operated in the READ mode with FILE and VERIFY options enabled.

AGE Interface can receive information from any General Purpose Parallel Interface of the SEEK BUS System. It employs three control signals, one status signal and twelve/sixteen lines for data. The control signals are the same as those used for input/output by DACTS. It uses one forty-two pin connector for input. The signal names associated with the pins of this connector are given in Table V. A System/4Pi CP-2 computer has three AGE connectors. The AGE Interface employs the signals associated with one of these three connectors. The connector used is the AGE JØ9 connector and the pin numbers associated with the signal names used by the AGE Interface are given in Table VI. Table VI also gives the function performed by each of these signals. Figures 16 and 17 give the timing diagram of the AGE signals used in LOAD and VERIFY modes, respectively.

AGE Interface has its own power supply for +5V. DACTS requires a power supply for ±5V. One such unit is shown with DACTS and AGE Interface in Figure 10. Figure 18 shows the input, output, erase and power connectors of DACTS. Figure 19 gives the function associated with each pin of DACTS power connector. Tables VII and VIII give the layout of DACTS and AGE Interface boards, respectively.

TABLE V

AGE Interface - Input

Signal Name	Winchester MRE 42 Pin Number	Description
IDLE H	J1 - DD	Shielded Twisted Pair
IDLE L	CC	
SHIELD	-	
DATA READY H	HH	Shielded Twisted Pair
DATA READY L	FF	
SHIELD	-	
DATA ACKNOWLEDGE H	LL	Shielded Twisted Pair
DATA ACKNOWLEDGE L	KK	
SHIELD	EE	
VERIFY MODE	AA	Twisted Pair
GROUND	BB	
DATA BIT ØØ	A	Single Wires
Ø1	B	
Ø2	C	
Ø3	D	
Ø4	E	
Ø5	F	
Ø6	H	
Ø7	J	
Ø8	K	
Ø9	L	
1Ø	M	
11	N	
12	P	
13	R	
14	S	
15	T	
DATA GROUND	U	
SHIELD	V	Overall Shield

TABLE VI

AGE Interface to System/4Pi CP-2 (JØ9) Connector

Pin Number	Signal Name	Source	Function	Description
1	GSOPTG	AGE*	GSE OPERATIONAL	Twisted Pair
5	GROUND	-	-	
6	GROUND	-	-	
7	SARGSE	AGE	SAR TO GSE	Twisted Pair with 11
9	GSBSAG	AGE	BUS TO SAR	Twisted Pair with 6
10	GSBSDG	AGE	BUS TO SDR	
11	GROUND	-	-	
12	GSRRG	AGE	READ RESTORE	Twisted Pair with 6
13	GSRCWG	AGE	READ COMPUTE WRITE	
14	GSWRTG	AGE	WRITE	
15	AGESP	AGE	AGE STORAGE PROTECT BIT	Twisted Pair
16	GROUND	-	-	
17	GSMB0	AGE	GSE BUS TO MAIN BUS (SIXTEEN BITS)	Twisted Pair
18	GSMB1	AGE		
19	GSMB2	AGE		
20	GSMB3	AGE		
21	GROUND	-	-	
22	GSMB4	AGE		
23	GSMB5	AGE		Twisted Pair
24	GSMB6	AGE		
25	GSMB7	AGE		
26	GROUND	-	-	
27	GSMB8	AGE		Twisted Pair
28	GSMB9	AGE		
29	GSMB10	AGE		
30	GSMB11	AGE		
31	GROUND	-	-	
32	GSMB12	AGE		Twisted Pair
33	GSMB13	AGE		
34	GSMB14	AGE		
35	GSMB15	AGE		
36	GROUND	-	-	
37	SYRSTG	AGE	SYSTEM RESET	
38	SINSMG	AGE	SINGLE INSTRUCTION MODE	
39	CGSMBG	AGE	GSE TO MAIN BUS	
40	GROUND	-	-	

*AGE represents AGE Interface

TABLE VI (continued)

Pin Number	Signal Name	Source	Function	Description
41	GROUND	-	-	
42	GSDA0	CP-2	SAR OR SDR TO AGE ON	
43	GSDA1	CP-2	THIS BUS (SIXTEEN BITS)	
44	GSDA2	CP-2		Twisted Pair
45	GSDA3	CP-2		
46	GROUND	-	-	
47	GSDA4	CP-2		
48	GSDA5	CP-2		
49	GSDA6	CP-2		Twisted Pair
50	GSDA7	CP-2		
51	GROUND	-	-	
52	GSDA8	CP-2		
53	GSDA9	CP-2		
54	GSDA10	CP-2		Twisted Pair
55	GSDA11	CP-2		
56	GROUND	-	-	
57	GSDA12	CP-2		
58	GSDA13	CP-2		
59	GSDA14	CP-2		Twisted Pair
60	GSDA15	CP-2		
61	GROUND	-	-	
64	GSPRBG	CP-2	SDR STORAGE PROTECT BIT	
65	PWRSG	CP-2	CP-2 POWER	Twisted Pair
66	GROUND	-	-	
67	GSBSYG	CP-2	STORAGE BUSY	
68	GROUND	-	-	Twisted Pair
69	STPKYG	AGE	STORAGE PROTECT KEY	
70	CP1GSG	CP-2	CP1 CLOCK	Twisted Pair
71	GROUND	-	-	
72	CP4GSG	CP-2	CP4 CLOCK	Twisted Pair
73	GROUND	-	-	

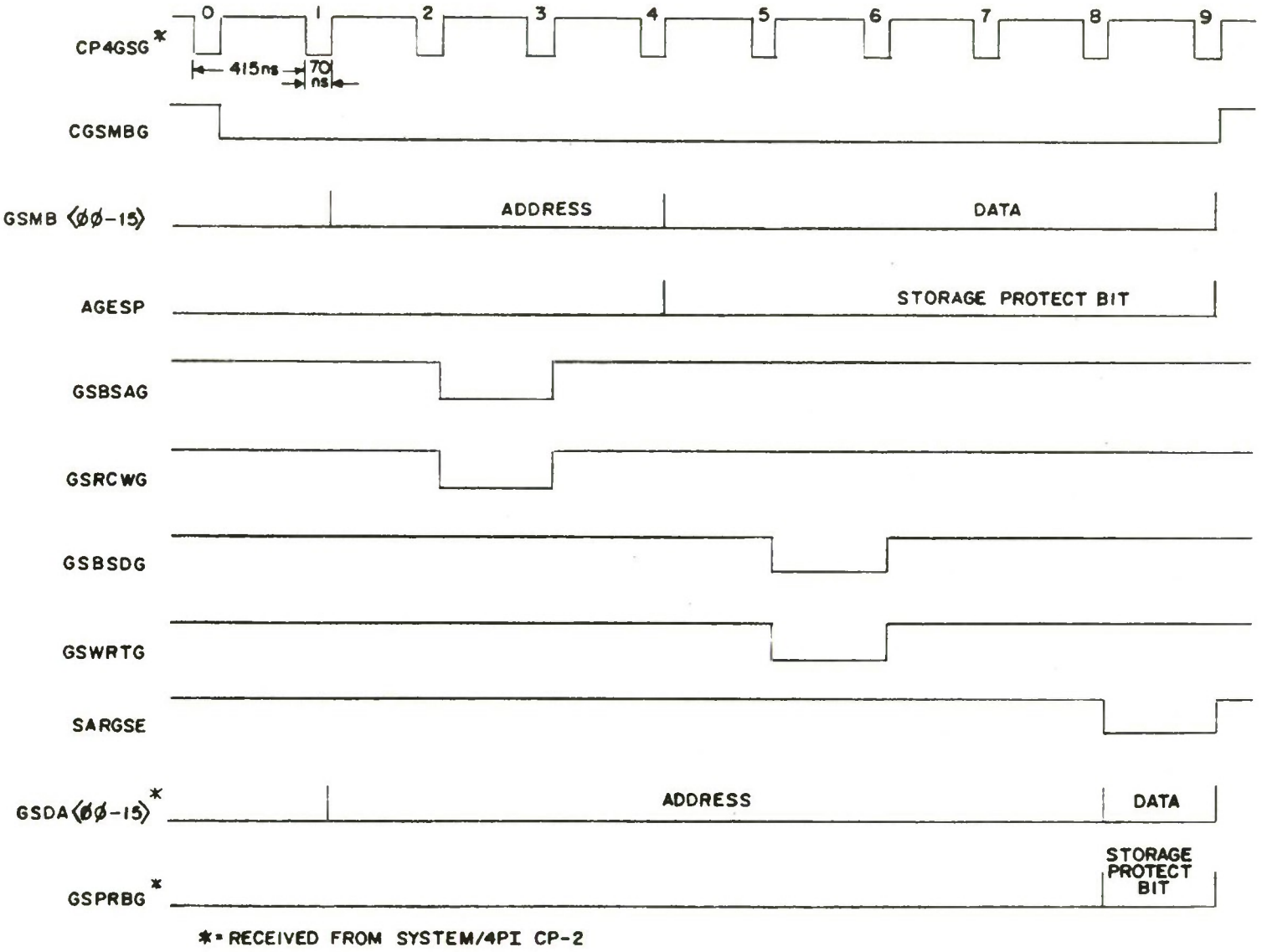
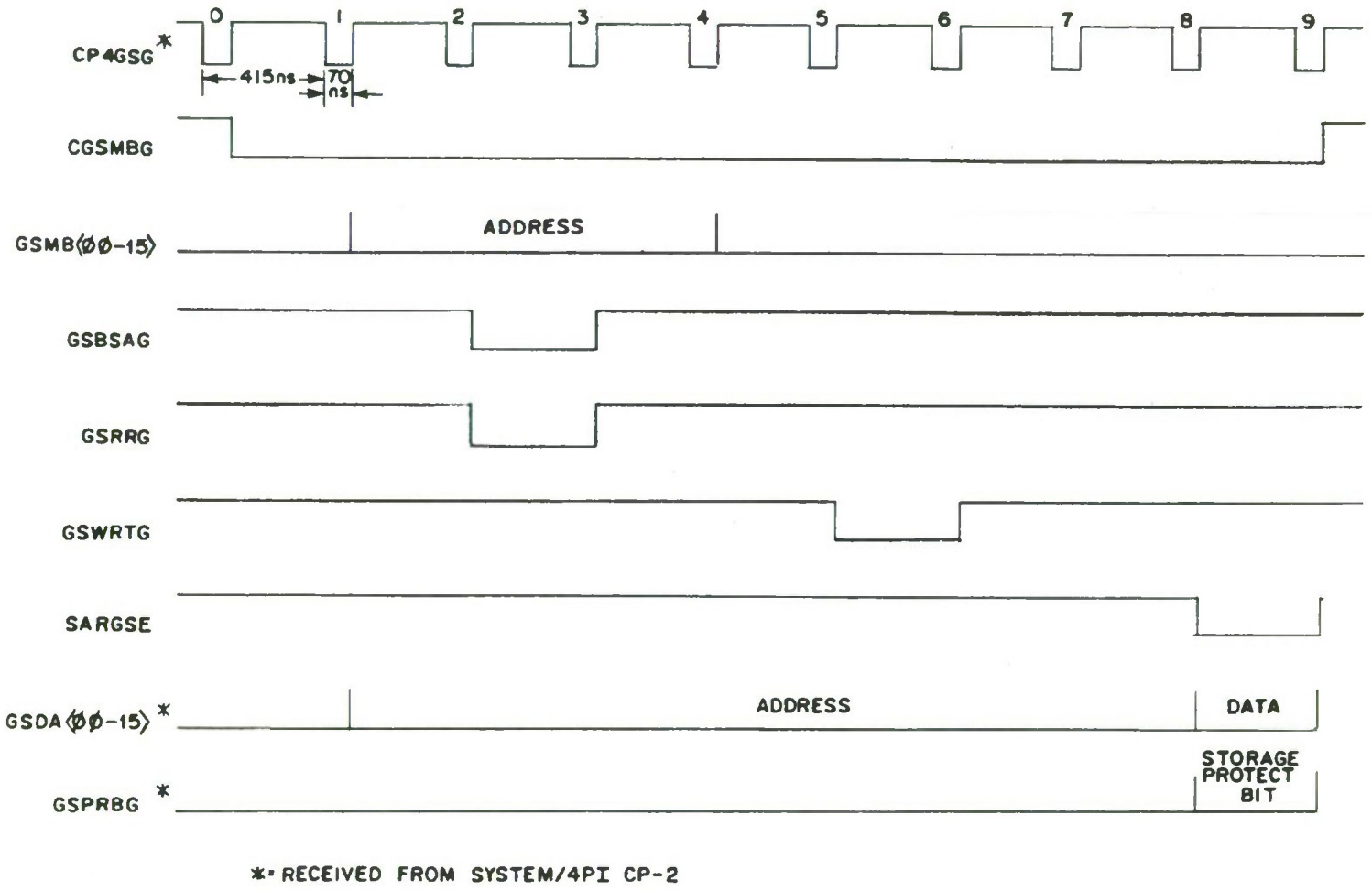


Figure 16 Timing Diagram to Load and Verify a Word



*: RECEIVED FROM SYSTEM/4PI CP-2

Figure 17 Timing Diagram to Verify a Word

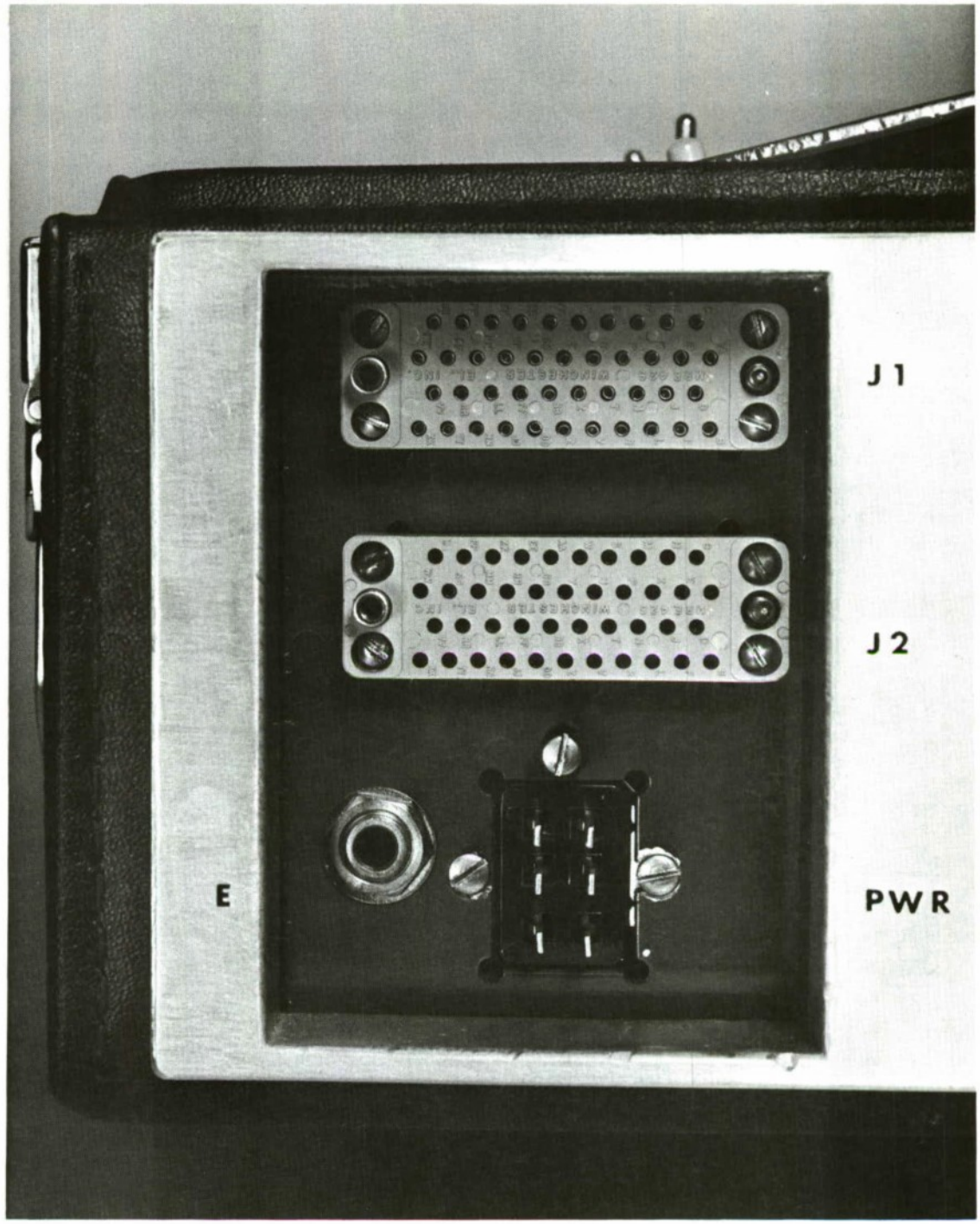
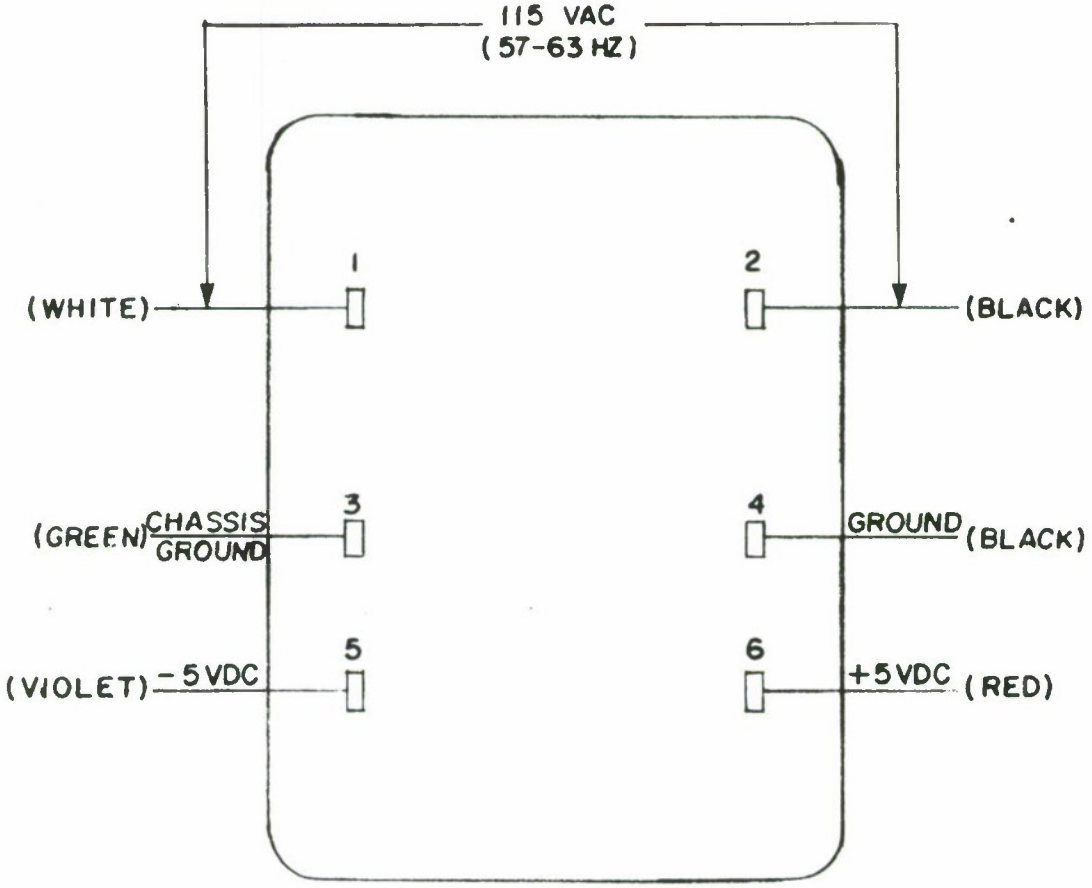


Figure 18 DACTS Connectors



(VIEW FROM INSIDE OF DACTS)

Figure 19 DACTS Power Connector

TABLE VII

Layout of DACTS Boards

Slot Number	BOARD				
	MC	WO	WS	RO	RI
1	S7400	S7408	S7486	S7495	F9322
2	S7402	S7408	S7486	S7495	F9322
3	S7400	S7408	S7486	S7495	F9322
4	S7400	S7408	S7486	S7495	F9322
5	S7410	S7410	S74193	S7495	S7400
6	F9602	S7476	S7400	S74193	S7400
7	S74121	S7451	F9324	S7495	-
8	S7408	S7404	S7410	S7408	F9615
9	S7410	S7495	S7476	S7408	F9615
10	S7400	S7408	F9602	S7402	F9614
11	S7404	S7408	S7408	S7400	F9614
12	S7400	S7486	S74121	S7400	-
13	S7410	S7495	F93403	S7495	S7495
14	S7404	S7495	F93403	S7495	S7495
15	S7430	S7495	F93403	S7495	S7495
16	S7476	S7495	F93403	S7495	S7495
17	S7400	S7404	S7476	S7495	S7404
18	CH16	S7476	S7410	S7476	S7408
19	CH16	S7451	F9324	S7476	-
20	S7400	S74193	S7476	S7400	-
21	S7404	S7495	S74121	S74121	CH16
22	S7476	S7420	CH16	S7404	CH16
23	S7476	S7402	S7476	S74193	F9602

TABLE VII (continued)

Slot Number	BOARD				
	MC	WO	WS	RO	RI
24	S7476	F9348	CH16	S7476	S7476
25	S7476	F7495	S7430	F9324	-
26	S7400	S7495	S7420	F9324	S7404
27	S7408	S7495	S7404	F9324	-
28	S7402	S7495	S7430	F9324	-
29	S7408	S7410	S7476	S7420	-
30	S7404	S7400	S7486	F9348	S7402
31	S74121	S7451	S7408	S7408	
32	F9602	S7408	S7402	S7404	F9602
33	F9024	S7495	S74121	CH16	F9602
34	S7476	S7476	F9602	F9602	CH16
35	F9602	S7404	S74121	S7476	CH16
36	S7408	S7404	S74121	S74121	S7408
37	S7476	S7476	S7400	S7402	F9602
38	S7408	S7404	S7408	S7400	CH16
39	S7400	S7400	F9338	S7408	S7476
40	S7476	S7476	F9338	CH16	-
41	S7476	S7404	S74193	F9602	-
42	S7400	S74121	S7476	F9348	-
43	S74121	S7451	CH16	S7486	-
44	CH16	S7451	S74121	S7476	CH16
45	S7476	S7495	CH16	S7404	-
46	F9602	S7408	S7404	S7430	-
47	CH16	S7451	S7476	S7408	-

TABLE VII (continued)

Slot Number	BOARD				
	MC	WO	WS	RO	RI
48	S7408	S7410	-	CH16	-
49	S74121	S7451	S7451	S7476	-
50	CH16	S7451	S7451	S7410	-
51	S74121	S7451	S7451	S7476	-
52	S7408	S7451	S7404	F9602	-
53	S7400	S7404	S74193	S7404	-
54	F9602	S7404	S7404	S7486	-
55	CH16	S7404	F9602	S7486	-
56	S74121	S7476	S74121	S7400	-
57	S7400	S7495	S74121	S74193	-
58	CH16	S7402	CH16	S7402	-
59	S74121	S74193	CH16	S7410	-
60	S7408	S7400	-	F9602	-

TABLE VIII

Layout of AGE Interface Boards

Slot Number	BOARD	
	GA	GB
1	F9324	F9312
2	F9324	F9312
3	F9324	S74193
4	F9324	F9615
5	S74H40	F9614
6	S74H40	S7442
7	S74H40	S74193
8	S74H40	S7476
9	S74H40	S74H40
10	S74H40	S74H40
11	F944	S74H40
12	S7408	S74H40
13	F9322	S7400
14	F9322	S7410
15	F9322	S7408
16	F9322	F9602
17	S7404	CH16
18	S7404	S7400
19	S7404	S7400
20	S74H40	S7476
21	S74H40	F944
22	S74H40	S7476
23	S7476	S7402

TABLE VIII (continued)

Slot Number	BOARD	
	GA	GB
24	S7476	S7404
25	S74193	S7402
26	S74193	S7476
27	S74193	S7476
28	S74193	S7404
29	S7404	S7404
30	S7402	S7476
31	S7400	S7408
32	S7408	S7476
33	S7410	S7404
34	S7400	S7400
35	S74193	S7400
36	S7404	S7476
37	F9322	S7400
38	F9322	S7400
39	F9322	S7476
40	F9322	S7400
41	F9322	S7408
42	S7476	CH16
43	S7408	CH16
44	S7400	S74H40
45	S7408	S7408
46	S7476	S7476
47	S7476	S74H40

TABLE VIII (continued)

Slot Number	BOARD	
	GA	GB
48	S7476	S74H40
49	S7495	F944
50	S7495	S7404
51	S7495	S7476
52	S7495	S7404
53	S7495	S7408
54	S7495	S7404
55	S7495	-
56	S7495	S7408
57	S7495	-
58	S7495	-
59	S7400	-
60	S7476	-

4.0 OPERATING PROCEDURE

Digital Avionics Cassette Transfer System may be used to write information on or to read information from a cassette. The read/write operations may be performed with several different options depending on a particular application. The selection of the mode of operation and the indication of the status of DACTS are done via a User/Status Panel shown in Figure 20. The different inputs available to a user are explained below (toggle switches are considered on in the "up" position and off in the "down" position):

SYS RESET: It resets the DACTS logic, clears all error indicators, resets the transport control circuit and when the pushbutton is released the tape is positioned to the Initial Load Point.

START: This pushbutton is used to initiate the operation of DACTS in the selected mode. If DACTS is initialized correctly and if any one of the available modes of operation is selected, then the GO indicator will turn on and DACTS will perform the function of the selected mode after the pushbutton is released.

MODE SELECTION: The Mode Selector rotary switch is used to select any one of the five basic modes of operation. Between any two mode selection settings there is an unused setting. If this switch is not set correctly then the GO indicator will turn on after the START pushbutton is released, but DACTS will not perform any function. The RAW indicator will be on if the Read After Write mode is selected.

I/O BITS: This toggle switch may be used to set the number of bits per I/O word to be used by DACTS. The on position of the switch indicates sixteen bits per word and the off position indicates twelve bits per word. The number of bits per word actually used by DACTS is determined by the second most significant bit of the file name received from an external device during Write/Read After Write mode, or read from the tape during Read mode. The I/O Bits switch may be used for user information only. If this switch is set incorrectly and if the File option is enabled then the I/O BITS ERROR indicator will turn on.

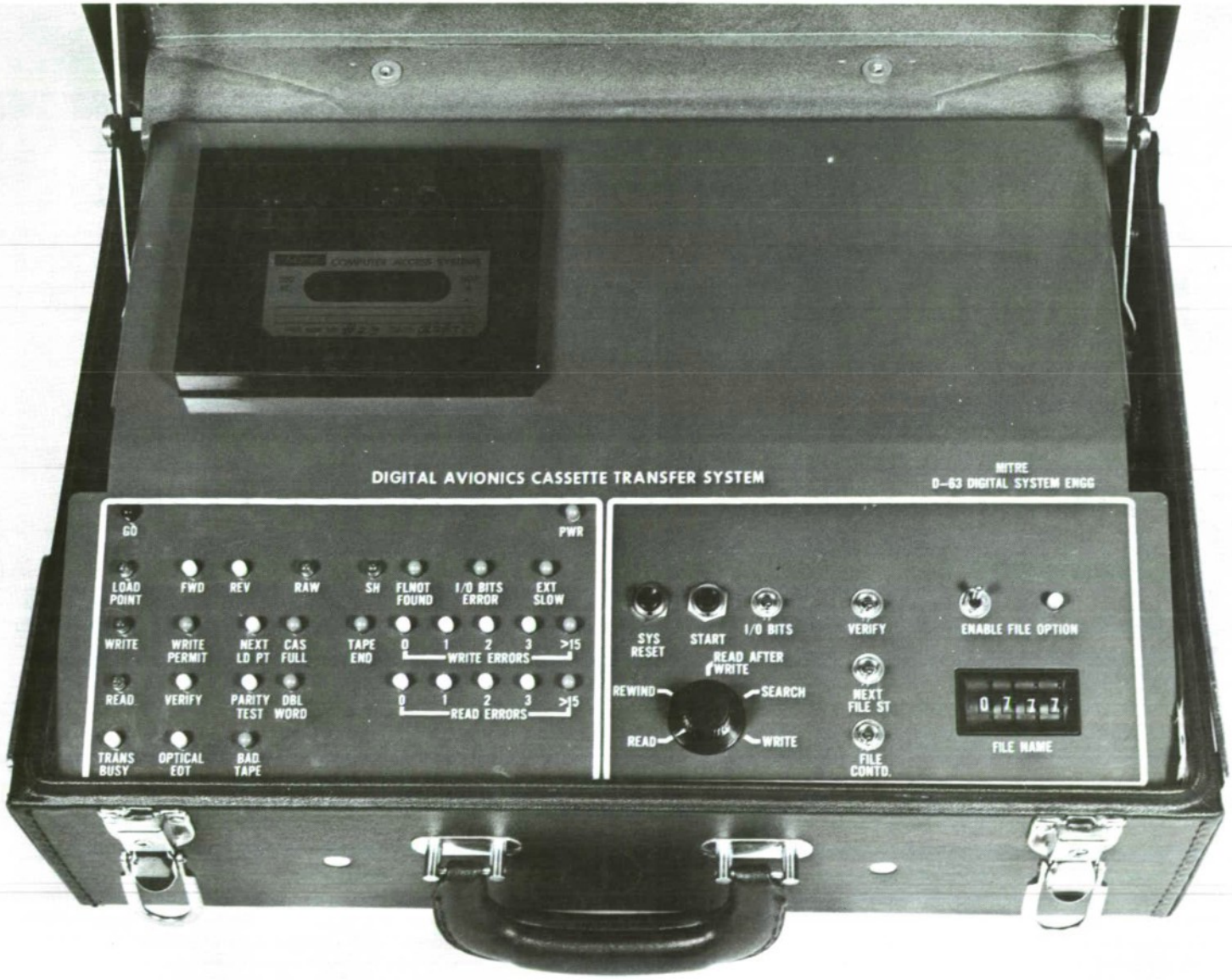


Figure 20 DACTS User/Status Panel

VERIFY: It may be used to enable the Verify option during a Read operation. The Verify option is enabled when the switch is in the on position.

NEXT FILE ST: It enables the Next Load Point option during a Write operation when it is set in the on position.

FILE CONTD: This switch should be in the on position if a file during a Write operation will be composed of more than one block.

ENABLE FILE OPTION: In the on position it enables the File option. When the File option is enabled the ENABLE FILE OPTION indicator will turn on.

FILE NAME: This thumbwheel switch can be used to set the file name as a four-digit binary coded octal number.

This completes the explanation of the different inputs available to the user. In any procedure, all the inputs may be given some value dependent on the mode of operation required, the system reset (by SYS RESET) and the operation initiated by START. During any mode of operation, the status of the unit is indicated on the User/Status Panel. These status indicators are explained below:

GO: It is turned on after START is released and it turns off at the end of the selected mode of operation. It can be reset by SYS RESET.

PWR: It is on when the unit receives +5V.

LOAD POINT: It is on when DACTS is in the Load Point mode and it is reset after the tape is positioned at the Initial Load Point or by SYS RESET.

FWD: It is on when a command for forward motion is given to the transport. This indicator is not used in the Load Point mode.

REV: It is on when a command for reverse motion is given to the transport. This indicator is not used in the Load Point mode.

RAW: It is on when the Read After Write mode is selected.

SH: It is on when DACTS is operating in Search mode and it turns off after the file is found or at the end of an unsuccessful search for a file through the whole tape.

I/O BITS ERROR: It will turn on if the I/O BITS switch is not set to the correct value and the File option is enabled. It may be reset by changing the value of I/O BITS input or by SYS RESET.

EXT SLOW: It is an error indicator that turns on in the Read/Read After Write mode if the external device has not accepted a word and DACTS is ready to send the next word. It indicates that a back up has occurred at the output of DACTS. It can be reset by SYS RESET.

WRITE: It is on when DACTS is in the Write mode and it can be reset by SYS RESET.

WRITE PERMIT: When on it indicates that the Write tab on the cassette has been removed and that no information can be written on the tape.

NEXT LD PT: It is on when the tape is being positioned to the next available Load Point. It is an option used in Write mode.

CAS FULL: When the Next Load Point option is enabled in Write mode, the tape is positioned to the next available Load Point. If information is stored on the whole tape and no space is available, then the CAS FULL indicator is turned on. It also turns on when all the available storage space on a cassette has been used up in Write mode. It can be reset by SYS RESET.

TAPE END: It turns on when the optical end of tape is encountered in either direction. It can be reset by SYS RESET.

WRITE ERRORS <Ø-3␣>15>: The number of errors occurring during a Write operation are indicated as a binary number by WRITE ERRORS <Ø-3>. WRITE ERROR Ø is the most significant bit of the error count. If the error count exceeds fifteen, then WRITE ERRORS >15 indicator turns on. This error counter can be reset by SYS RESET.

READ: It is on when DACTS is in READ mode. It turns off at the end of Read mode (file end if File option is enabled, else tape end). It can be reset by SYS RESET.

VERIFY: It is on during the Verify portion of Read-Verify mode. It can be reset by SYS RESET.

FL NOT FOUND: Indicates missing file. It can be reset by SYS RESET.

PARITY TEST: It turns on if a parity test is required during a Read operation. It indicates that the two groups of bits representing the same word are not equal when read off the tape. A check of the odd parity is made to determine which one of the two groups of bits gives the correct word. This test gives the correct word if only one of the forty-two/fifty bits is incorrect. It can be reset by SYS RESET.

DBL WORD: It turns on if both the words obtained from the two unequal groups of bits recorded on the tape to represent a word satisfy the odd requirement on a read. It indicates that at least two of the forty-two/fifty bits for the word are incorrect. It gives the correct word if no errors occurred in reading the second group of bits. It is an error condition and can be reset by SYS RESET.

READ ERRORS <Ø-3␣>15>: The number of errors occurring during a Read operation are indicated as a binary number by READ ERRORS <Ø-3>. READ ERROR Ø is the most significant bit of the error count. If the error count exceeds fifteen, then READ ERRORS >15 indicator turns on. These indicators can be reset by SYS RESET.

TRANS BUSY: It is on if the transport is busy; i.e., the tape is in motion.

OPTICAL EOT: It turns on when the Optical End of Tape is encountered and the unit is not in the Load Point mode/resetting to Initial Load Point. It can be reset by SYS RESET.

BAD TAPE: It turns on if clock pulses are not received from the transport and the tape is not at its physical end. It indicates one or more of the following conditions:

(i) Cassette is not mounted correctly;
(ii) Tape is broken;
(iii) Clock track is missing;
(iv) Insufficient oxide on the tape.

This error indicator can be reset by SYS RESET.

ENABLE FILE OPTION: It is on if the File Option is enabled.

The indicators explained above give sufficient information to determine the status of DACTS during any mode of operation. DACTS uses two connectors to interchange information with external units.

It also has an erase socket and a power connector. These are located on the right side of the unit and are shown in Figure 18. The top connector is the J1 connector used for input; the second connector is the J2 output connector; and the six pin connector is used for power. The socket to the left of the power connector is used for erase.

DACTS can be operated in ten different modes. A unique set of values of user inputs have to be used for each mode, but the general procedure to operate DACTS is similar for all modes. This operating procedure is shown in Figure 21. Turn off the power for all units used and make all the interconnections. Turn on the power. Reset DACTS and mount the cassette in place. Reset DACTS and set up the user inputs for the mode of operation required. Reset DACTS again and push START when the transport is not busy. GO will turn on and DACTS will operate in the selected mode. At the end of operation, reset DACTS and remove cassette or initiate a new operation after the transport is not busy. When DACTS is not being used remove the cassette and turn off the power. The cassette should never be left mounted on the transport when DACTS power is turned on or off.

The AGE Interface has user inputs, status indicators and two connectors on the User/Status Panel. The user inputs are explained below:

START: When pushed, it resets the AGE Interface logic and on release the AGE Interface initializes to perform the functions of the selected mode if clock pulses are being received from the System/4Pi CP-2 computer.

LOAD: In the on position it enables the Load mode.

VERIFY: In the on position it enables the Verify mode.

4π SYSRST: It sends a reset pulse to System/4Pi CP-2. On receiving a reset System/4Pi CP-2 starts program execution from location zero if any executable program exists in its memory.

PWR: It is the power switch for the AGE Interface. When turned on it forces System/4Pi CP-2 into Single Instruction mode (halting execution of any program).

The User/Status Panel has seven status indicators. They are:

GO: It turns on when the first word of a block of information to load data into System/4Pi CP-2 memory is received. It resets when START is pushed.

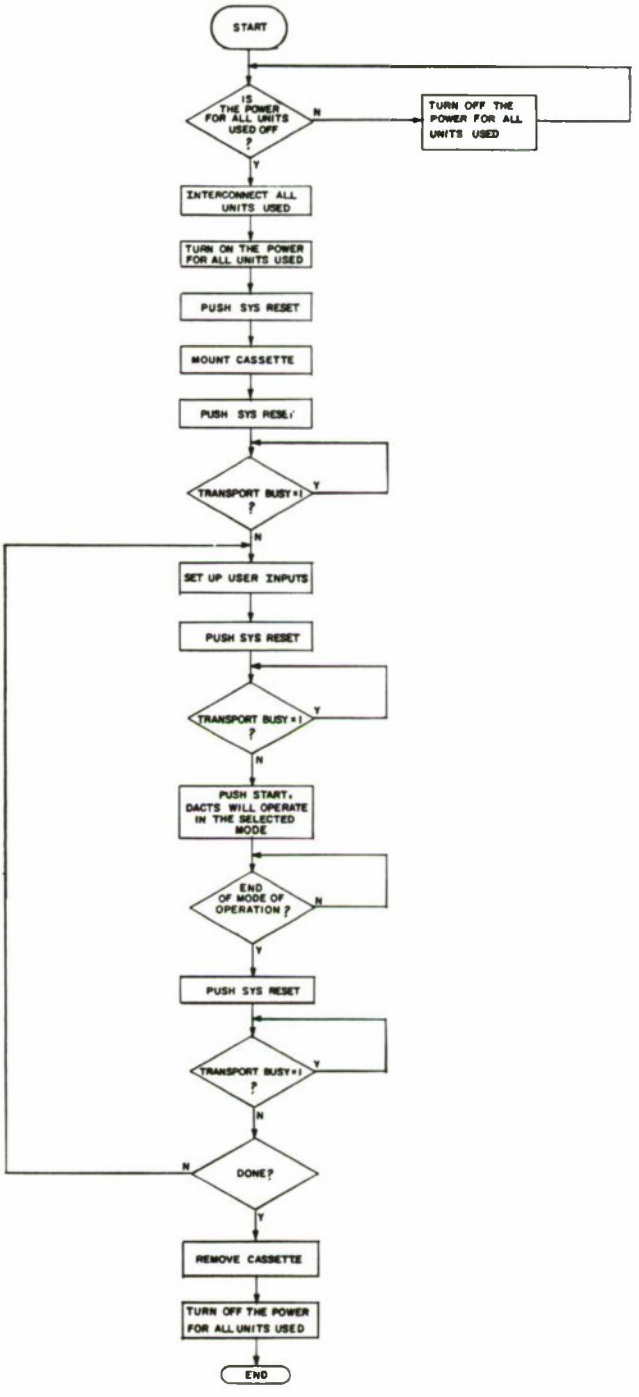


Figure 21 General Operating Procedure for DACTS

LOAD: It turns on when the unit is in Load mode and it resets when START is pushed.

VERIFY: It turns on when the unit is in Verify mode and it resets when START is pushed.

ERROR: SAR turns on when an address comparison error occurs in Load/Verify mode. SDR turns on when a data comparison error occurs in Load/Verify mode. These error indicators reset when GO turns on.

4π STORAGE BUSY: It is on when System/4Pi CP-2 storage is busy, and it indicates that a stored program is being executed.

PWR: It is on when the unit is receiving +5V.

The user panel has two connectors. They are:

TO EXT DEVICE: It is an input connector through which the AGE Interface receives information from an external device.

TO SYSTEM/4π: It is used to connect the AGE Interface to the System/4Pi CP-2 AGE connector JØ9.

AGE Interface can be used in three different modes of operation. The operating procedure for the three modes of operation are similar and it is given in Figure 22. To operate the AGE Interface in Load, Verify or Load-Verify mode, the power for all systems (external device, AGE Interface and System/4Pi CP-2) should be off, initially. Next, appropriate interconnections are made and then AGE Interface and external device power is turned on followed by power on for System/4Pi CP-2. The user inputs are set up and START is pushed. In the pushed position START resets the AGE Interface. When released the AGE Interface initializes to operate in the selected mode. At the end of operation of the AGE Interface in the selected mode, System/4Pi CP-2 can be reset by 4π SYSRST. To reuse AGE Interface, set up the user inputs and push START if System/4Pi CP-2 storage is not busy. To reuse AGE Interface when System/4Pi CP-2 storage is busy turn System/4Pi CP-2 and AGE Interface power off (in that order). Then turn AGE Interface and System/4Pi CP-2 power on (in that order). This will force the computer into Single Instruction mode. The user inputs for the required mode of operation can then be set up and the operation initiated by pushing START. This procedure may be followed to utilize AGE Interface with any external device with output compatible with AGE Interface input.

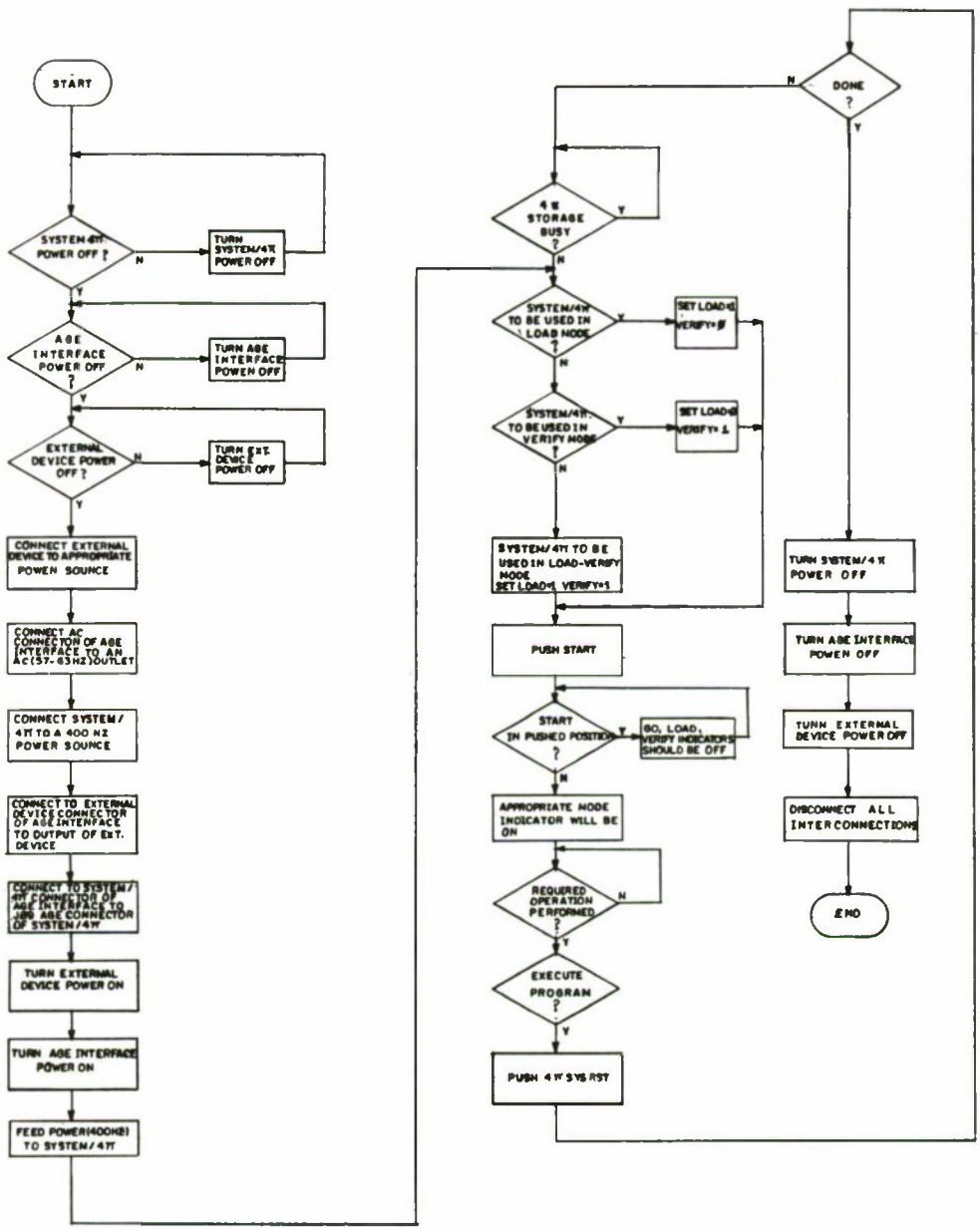


Figure 22 AGE Interface Operating Procedure

The procedures described above for DACTS and AGE Interface may be combined to store information on a cassette and to load System/4Pi CP-2 software. The alternate program loading procedure consists of two different operations. The first operation involves the storage of information on a cassette, and the second operation includes the reading of information from the cassette by DACTS and the storage of data into System/4Pi CP-2 memory by AGE Interface. These operating procedures are explained below:

Operating Procedure to Load Information on a Cassette Using DACTS and PDP-8 Minicomputer Equipped with a Magnetic Tape Transport, a Data Buffer, a Teletype (TTY) and a Paper Tape Reader (see Figures 7 and 9)

1. Connect the units as follows:

   a) AC connector of DACTS supply unit to 105-132 VAC (57-63 Hz) outlet.

   b) The output of DACTS supply unit to the power connector (6-pin connector at the bottom right) of DACTS.

2. Turn DACTS and PDP-8 system power on.

3. Initialize DACTS as follows:

   a) Push SYS RESET.

   b) Insert cassette into the transport with Side A up.

   c) Push SYS RESET and wait until transport is not busy.

4. To erase a cassette, do the following (a cassette must always be erased if recording is required from the Initial Load Point):

   a) Insert erase plug into its socket.

   b) Set the mode selection switch for WRITE/READ AFTER WRITE.

   c) Set all toggle switches in the Ø position.

   d) Push START. The cassette erase process will start. GO, WRITE, FWD and TRANS BUSY indicators will be on.

e) The operator can halt the erase process by removing the erase plug from its socket.

f) If not stopped by the operator, the erase process will continue until the whole tape has been erased and TAPE END turns on. Remove the erase plug.

g) At the end of erase, FWD and TRANS BUSY will turn off.

h) Push SYS RESET and wait until transport is not busy.

5. Set the mode selection switch for READ AFTER WRITE, NEXT FILE ST=1, FILE CONTD=1, and all other switches in the Ø position. RAW indicator will be on. Push SYS RESET. Wait until transport is not busy.

6. Push START, GO will turn on. The transport will move to the next available load point (Initial Load Point if the cassette is blank). During this process NEXT LD PT and TRANS BUSY will be on. FWD or REV will be on depending on the direction of motion. If the cassette does not have any space available for recording then CAS FULL indicator will turn on. In that case, push SYS RESET. Wait until transport is not busy. Remove this cassette. Use another cassette and go to 3.

   When positioned at the load point, WRITE will turn on and DACTS will be ready to record received information on the cassette.

7. For PDP-8 System:

   If the Cassette Generator Program is already loaded then go to h, else:

   a) Depress STOP. Set TTY mode selection switch to "on line."

   b) Set Switch Register (SR) = ØØ776Ø. Depress LOAD ADDRESS.

   c) Depress START. Wait until TTY bell rings.

   d) Depress STOP. Load Cassette Generator Program paper tape into PDP-8 paper tape reader.

e) Set SR = Ø17777. Depress LOAD ADDRESS.

f) Set SR = Ø13777. Depress START. The paper tape will feed through the reader. When the reading stops the binary loader will halt. If Link = 1 and Accumulator = ØØØØ then go to 7(g), else go to 7(d).

g) Mount the magnetic tape generated by the 8PI Assembler on Tape Drive #1. Depress RESET, LOAD REWIND and then REMOTE on Tape Drive #1. Wait until REMOTE turns on. If REMOTE does not turn on, then depress RESET and do this step again.

h) Depress STOP.

i) Set SR = ØØ7ØØ1 if DB8A is used
or SR = ØØ7ØØ2 if DB8B is used
or SR = ØØ7ØØ4 if DB8C is used

Depress LOAD ADDRESS.

Set SR = ØØØØ2Ø to use DACTS Test Program, else
Set SR = ØØØØØ.

j) Depress START. The Cassette Generator Program will be executed. The program communicates with the user through the TTY. The user has to type in the three octal digit File Name at the beginning of the file. For each partition, the program types the partition title and gives the user the option to bypass that partition. If bypassed, the program goes to the next partition. If the partition is not bypassed then the user has the option to generate information for BSS's in the System/4Pi CP-2 program. The program reads the partition and stores the assembled information in an output buffer.

If the output buffer gets full then the information is written on the cassette and read back. If the end of the partition is reached then partition and cumulative checksums are typed on the TTY and the information is written on the cassette. During write, the information will also be read back. This process will halt after all partitions have been read or if an error occurs.

Figure 23 shows a sample user-program conversation. While a partition is being written and read back the READ, FWD, and TRANS BUSY indicators will also turn on. Errors detected by DACTS will be displayed by WRITE ERRORS <Ø-3>␣15>, PARITY TEST, DBL WORD, and READ ERRORS <Ø-3>␣15> indicators on the user panel.

8. At the end of the write process push SYS RESET. Wait until transport is not busy.

9. After each file is recorded on the cassette its presence on the tape may be verified as follows:

   a) Set mode selection switch for SEARCH, ENABLE FILE OPTION = 1 and FILE NAME = name of the file recorded.

   b) Push START. DACTS will search for the file and will halt when found.

   c) If not found the FLNOT FOUND indicator will turn on. This indicates an error.

   d) Push SYS RESET. Wait until the transport is not busy.

10. If errors occur during generation of a file then:

   a) if erroneous file starts from the Initial Load Point then go to 4.

   b) else, (i) set DACTS mode selection switch for READ, ENABLE FILE OPTION = 1 and FILE NAME = name of the file that precedes the erroneous file on the cassette;

      (ii) push START. Wait until the Read mode ends;

      (iii) go to 4.

11. To record a different file on the same cassette, do as follows:

   a) dismount the magnetic tape from Tape Drive #1 as follows:

      (i) push UNLOAD. The tape will rewind and the drive cover will open;

```
FILE NAME OCTAL DDD
RESET CASSETTE
0777[1]

AWACS SID GROUND PROGRAM
BYPASS PARTITION? Y OR N?
N
WRITE BSS'S? Y OR N?
Y
Ø[2]
PARTITION CHECKSUM IS ØØ58137A
CUMULATIVE CHECKSUM IS ØØ58137A
Ø

SID INTERRUPT PARTITION
BYPASS PARTITION? Y OR N?
Y

MATH PARTITION
BYPASS PARTITION? Y OR N?
Y

[3]
BYPASS PARTITION? Y OR N?
Y

AWACS SID RAD MSG CREATE
BYPASS PARTITION? Y OR N?
N
WRITE BSS'S? Y OR N?
N
PARTITION CHECKSUM IS 13F62D2D
CUMULATIVE CHECKSUM IS 13AE3E57
Ø

AWACS SID MANUAL INPUT
BYPASS PARTITION? Y OR N?
Y

RADIO MSG PARTITION
BYPASS PARTITION? Y OR N?
Y

AWACS SID INTERCOMPUTER
BYPASS PARTITION? Y OR N?
Y

SHORT TIMER
BYPASS PARTITION? Y OR N?
Y

END OF PROGRAM
```

User responses are underlined.

[1]File Name

[2]Ø indicates that no errors were detected.

[3]This partition does not have a title.

Figure 23 A Sample User-Program Conversation

(ii) remove the tape.

b) go to 5.

12. To record the same partition on a different cassette do as follows:

a) Remove the cassette from the transport.

b) Insert the next cassette into the transport.

c) Push SYS RESET. Wait until transport is not busy.

d) Go to 4.

13. When done do the following:

a) Push STOP on the PDP-8;

b) Dismount the magnetic tape from Tape Drive #1 as follows:

(i) push UNLOAD. The tape will rewind and the drive cover will open;

(ii) remove the tape.

c) Remove the cassette from the transport.

d) Turn DACTS power off.

The information stored on the cassette can be read and loaded into System/4Pi CP-2 memory via AGE Interface, but this procedure requires that the computer's memory be cleared first. This may be done by a Clear Core Program, and this program may be loaded into System/4Pi CP-2 memory and executed before any other program is loaded. The Clear Core Program may be recorded as the first file on every cassette. (NOTE: The Clear Core Program should not be employed if the information to be loaded into System/4Pi CP-2 memory is used to "patch up" the existing data.)

Operating Procedure to Load System/4Pi CP-2 Using DACTS and AGE Interface (see Figures 8 and 10)

1. Verify that the power for DACTS, AGE Interface and System/4Pi CP-2 is off.

2. a) Connect AC connector of DACTS supply unit to a 105-132 VAC (57-63 Hz) outlet.

   b) Connect the output of DACTS supply unit to the power connector of DACTS (6-pin connector at the bottom right).

   c) Connect AC connector of AGE Interface to a 105-132 VAC (57-63 Hz) outlet.

3. Connect DACTS, AGE Interface and System/4Pi CP-2 as follows:

   a) "J2" connector (second from top) of DACTS to "TO EXT DEVICE" connector of AGE Interface.

   b) "TO SYSTEM/4π" connector of AGE Interface to "JØ9" AGE connector of System/4Pi CP-2.

4. Turn DACTS and AGE Interface power on.

5. Turn System/4Pi CP-2 power on (turn Control/Display Unit power on and set it for Computer mode).

6. Push SYS RESET of DACTS.

7. Insert the cassette into the transport with Side A up (if the appropriate cassette is not already in place).

8. Push SYS RESET of DACTS. Wait until transport is not busy.

9. a) Set LOAD = 1 and VERIFY = Ø for AGE Interface.

   b) Push START pushbutton of AGE Interface. In the "pushed" position GO, LOAD and VERIFY indicators will be off and when released LOAD indicator will turn on.

10. For DACTS:

    a) Set the mode selection switch for READ, ENABLE FILE OPTION = 1, FILE NAME thumbwheel switch = four octal digits of file name and all other user inputs = Ø. (I/O BITS = Ø for 12 bits per word.)

    b) Push SYS RESET and wait until transport is <u>not</u> busy.

    c) Push START. The transport will move forward in Search mode. GO, SH, FWD and TRANS BUSY will be on.

    d) If the file is not found then FLNOT FOUND for DACTS will turn on. It indicates that the required file is not on the cassette or the File Name is wrong. Then do the following:

        (i) push SYS RESET. Wait until transport is <u>not</u> busy;

        (ii) change the File Name or the cassette;

        (iii) go to 7.

    e) When the file is found READ will turn on and SH will turn off and the file will be read. When DACTS goes to Read mode the GO indicator for AGE Interface will turn on and information will be stored into System/4Pi CP-2 memory. The AGE Interface errors will be indicated by SAR (Storage Address) and SDR (Storage Data) indicators.

        DACTS errors will be indicated by PARITY TEST, DBL, WD and READ ERRORS <Ø-3>␣15>.

    f) At the end of Read mode, GO, READ, FWD and TRANS BUSY indicators will turn off.

11. If any errors occur then go to 8.

12. If no errors then push SYS RESET for DACTS. Wait until transport is <u>not</u> busy.

13. If System/4Pi CP-2 is loaded with the Clear Core Program then do the following:

a) Push 4π SYS RESET (AGE Interface). The 4π STORAGE BUSY will turn on. Wait until System/4Pi CP-2 storage is not busy.

b) Go to 8.

14. If done then do the following:

a) Remove cassette from the transport.

b) Turn System/4Pi CP-2 power off (set the Control/Display Unit to LOCAL mode).

c) Turn off the power for DACTS and AGE Interface.

d) Disconnect all interconnections.

NOTE: When using AGE Interface with System/4Pi CP-2, it is very important that the System/4Pi CP-2 power is off whenever the AGE Interface power is turned on/off.

The two operating procedures given above constitute the alternate program loading method for System/4Pi CP-2. Any system employing DACTS and/or AGE Interface in different modes of operation can follow the above procedures with some variations.

5.0 MAINTENANCE

Digital Avionics Cassette Transfer System requires preventive maintenance for the magnetic heads. The frequency of cleaning the magnetic heads depends on the amount of usage and the operating environment. For light usage in a clean environment, heads should be cleaned once a week. When usage is heavy and environment is unclean, heads should be cleaned once a day or once every 100 tape passes. Any brand name head cleaner or Freon or Isopropyl Alcohol may be used to clean the heads with an ordinary hygienic cotton tipped applicator. Apply cleaning solution to transport head and other parts of the transport that come in contact with the tape. Remove excess solution at once. Use the unit only after the chemical has dried. There should be no residue on the heads after cleaning.

DACTS does not require any other preventive maintenance. The hardware may be checked periodically by using DACTS Test Program. DACTS Test Program is a subroutine of the Cassette Generator Program used to load information on a cassette. The procedure to operate the DACTS Test Program is the same as the operating procedure to load information on a cassette explained in Section 3.0, with the exception that 7(i) should have an additional operation viz. Set SR = ØØØØ2Ø after Depress LOAD ADDRESS. In this program information sent to DACTS, and that received from it, is printed on the high speed printer if input and output words are not the same. This program can only indicate the existence of errors. It is not recommended for troubleshooting DACTS. To troubleshoot for possible hardware faults, DACTS/AGE Interface Test Unit (DATU) should be used. It has user inputs and status indicators. They are (all toggle switches represent a 1 in "up"/on position and a Ø in "down"/off position):

DATA BITS: These toggle switches can be used to set up the output word. Twelve/sixteen bits may be set up depending on the word length used.

WORD LENGTH: This input is used to indicate the word length used. In the on position it indicates sixteen bits per word and data bit Ø1 of the first output word after START is a 1. In the off position, it indicates twelve bits per word and data bit Ø1 of the first output word after START is a Ø.

START: This pushbutton can be used to initiate an output message.

RESET: It can be used to reset the test unit. It can also be used to indicate the end of an output message.

ON/OFF: It is used to turn the test unit power on/off.

IDLE: When on, it indicates than an output message is being generated.

READY: It indicates the status of the Output Ready signal of the DATU.

ON: When on, it indicates the presence of +5V.

DACTS/AGE Interface Test Unit has an output connector on the right side.

Operating Procedure to Troubleshoot DACTS Using DATU

1. Connect DACTS input connector to DATU output connector.

2. Turn DATU power on.

3. Turn DACTS power on.

4. Push DATU Reset.

5. Initialize DACTS as follows:

   a) Push SYS RESET.

   b) Insert cassette into transport with Side A up.

   c) Push SYS RESET and wait until transport is not busy.

   d) If desired, the cassette may be erased using the procedure described in Section 3.0.

6. Set mode selection switch for WRITE, FILE CONTD = Ø/1 depending on part of hardware tested, and all other switches in the Ø position. Push START. GO and WRITE will turn on.

7. Set up DATA BITS and WORD LENGTH. Push RESET.

8. Push START (DATU). IDLE will turn on and remain on for the duration of output message. READY will be on at reduced intensity as it follows Output Ready. The cassette should move forward in Write mode. FWD and TRANS BUSY will be on.

9. Information will be written on the tape by the Write circuit, read back by the Read Circuit and checked by the Write-Verify circuit. This process will continue until DATU RESET/DACTS SYS RESET is pushed.

The arrangement explained above utilizes most of DACTS hardware and can be used to isolate and identify hardware faults.

DACTS utilizes TTL/Monostable Multivibrators, and the pulse timing of most of them can vary by 50% without affecting the normal operation of DACTS. Some of these multivibrators are very critical. The pulse duration of these should never vary by more than 20%. These critical multivibrators with their minimum required pulse duration are listed in Table IX. One of the components of DACTS is a cassette transport, and Table X lists some of the easily identifiable symptoms of faulty transport with possible solutions.

AGE Interface does not require any regular maintenance. Periodic testing of hardware is recommended. A quick test involves loading of System/4Pi CP-2 from an AGE test cassette using a DACTS and verifying the checksum on the Control/Display Unit. Troubleshooting of faulty AGE Interface may be done with the DACTS/AGE Interface Test Unit. DATU may be used to load data into a System/4Pi CP-2 memory location via AGE Interface.

Operating Procedure to Troubleshoot AGE Interface Using DATU

1. Verify that power for DATU, AGE Interface and System/4Pi CP-2 is off.

2. a) Connect output connector of DATU to "TO EXT DEVICE" connector of AGE Interface.

   b) Connect "TO SYSTEM/4π" connector of AGE Interface to "JØ9" AGE connector of System/4Pi CP-2.

TABLE IX

Critical DACTS Multivibrators

Board	Multivibrator		Minimum Pulse Duration	Function
	Location	Pin Number		
MC	06	09	50 ms	INITIAL LOAD POINT END
MC	07	06	250 ms	FILE GAP (WRITE)
MC	35	06	100 ms	NEXT LOAD POINT CONTROL
MC	46	06	100 ms	NEXT LOAD POINT CONTROL
MC	46	10	315 ms	NEXT LOAD POINT CONTROL
MC	51	06	250 ms	FILE GAP (WRITE)
MC	54	10	315 ms	NEXT LOAD POINT CONTROL
MC	59	06	315 ms	NEXT LOAD POINT CONTROL
WS	35	06	10.4 µs	WRITE CLOCK
WS	36	01	10.4 µs	WRITE CLOCK
RO	34	10	220 µs	WORD GAP (READ)
RO	60	06	2 ms	BLOCK GAP (READ)
RI	33	06	180 ms	FILE GAP (READ)
RI	37	06	50 ms	BLOCK START (WRITE)
TC*	A10	07	7.5 µs	SPEED CONTROL (FAST)
TC*	A10	09	30 µs	SPEED CONTROL (SLOW)

* Tape Controller

TABLE X

Symptoms and Solutions for Transport Problems
(Operation and Interface Manual for MFE Model 250C)

SYMPTOM	SOLUTION
I. Tape Motion 1) No motion	1) No Servo voltage applied or current limited 2) Cassette not properly loaded in transport 3) Speed Control One-Shot normally in wrong state 4) Motor terminals inadvertently shorted out 5) Tape bound up
2) Incremental motion-tried to start but will not continue in either direction	1) Tape Speed Control Clock or analog clock test point inadvertently grounded 2) No clock track on tape 3) Cassette upside down 4) Servo voltage low, or current limited 5) Both motion commands present
3) Erratic Motion, tape moves, but jerky in either direction	1) Both motion commands present 2) Cassette upside down 3) Dirty Heads

TABLE X (continued)

SYMPTOM	SOLUTION
	4) Bad tape
	5) Speed Control One-Shot normally in wrong state
4) No Forward Motion	1) Forward command not held at +5 volt level
	2) Tape bound up
5) No Reverse Motion	1) Reverse command not held at +5 volt level
	2) Tape bound up
6) Inability to change speeds	1) Speed Control One-Shot not functioning
II. Data Lines 1) No Data	
A) Data not being written	1) Write permit tab missing
	2) Write permit inadvertently tied to a +5 volt
	3) Head wires loose
B) Data not being read	1) Analog data test point or data output line(s) grounded inadvertently
2) Wrong Polarity	1) Flux 1 & Flux 0 lines reversed
	2) Data (+) Data (-) lines reversed

TABLE X (continued)

SYMPTOM	SOLUTION
3) Erratic Data	1) Dirty Heads 2) Bad Tape 3) Not stopping in IRG 4) Not waiting until tape is up to speed before writing 5) Cassette does not have a pressure pad
III. Status Condition 1) Busy-present where no tape motion not present with tape motion	1) Busy line tied to +5 volts erroneously 2) Busy line tied to 0 volts erroneously
2) EOT - present at all times	1) Transport not reset by momentarily grounding RESET line 2) EOT line tied to +5 volts erroneously
3) EOT - Not present at end of tape	1) EOT line tied to ground erroneously

3. Turn DATU and AGE Interface power on.

4. Turn System/4Pi CP-2 power on (turn Control/Display unit power on and set it for computer mode).

5. Push RESET of DATU.

6. For AGE Interface:

   a) Set LOAD and VERIFY to appropriate values.

   b) Push START (in the "pushed" position GO, LOAD and VERIFY indicators will be off and when released one of the mode indicators will turn on).

7. For DATU:

   a) Set up DATA BITS with bit ØØ = Ø, bit Ø1 = 1, bit Ø6 = 1, bit Ø7 = Storage Protect Bit and remaining bits can either be Ø or 1.

   b) Set Word Length for twelve bits per word.

   c) Push START (DATU). DATU will generate an output message and AGE Interface will load <DATA BIT<Ø8-11>␣<ØØ-11>> with Storage Protect Bit = <DATA BIT Ø7> at location <DATA BIT<Ø2-11>␣<ØØ-Ø5>>.

8. This process will continue until DATU RESET/AGE Interface START are pushed.

The procedure explained above utilizes all of AGE Interface hardware and the functioning of all signals can be checked and faults isolated by this method. A combination of test procedures explained above may be used to test and/or verify AGE Interface hardware. The test method employing DATU can troubleshoot the hardware and checksum verification using DACTS can verify it.

The test procedures employing DATU explained above can also be performed using a PDP-8, PDP-8/I or PDP-8/E minicomputer equipped with a Data Buffer. Programs have been developed to test/troubleshoot DACTS/AGE Interface using any one of the above mentioned minicomputers. These test procedures are not required and methods employing a DATU are recommended.

6.0 HARDWARE DESCRIPTION

Digital Avionics Cassette Transfer System is composed of five EC60 type boards. It has about two hundred and fifty TTL/MSI circuit packages. Age Interface is composed of two EC60 type boards with about ninety TTL/MSI circuit packages. This section describes the hardware functioning of these units. Every attempt is made to explain the hardware without going into details about every signal. The hardware is described with the aid of flow charts and sufficient details are explained to enable the reader to understand the logic circuit.

The logic circuit for DACTS is divided into six different parts and each part performs a specific function. These functions are: Master Control, Read, Write, Write Verify, Search and Input/Output. The Master Control includes the circuit for Mode Control, Rewind, Verify and Next File Start. The hardware description is also divided according to the logic circuit division. Each logic circuit division is explained by a different set of flow charts and the description for different options for a mode of operation is included with the description for that mode. Only the Mode Control section of Master Control is explained separately.

When power is turned on the signals are not reset and a system reset is required by the user to disable all signals. After the cassette is loaded in place, it should be positioned to the Initial Load Point. Once the cassette is at the Initial Load Point, DACTS can be operated in any mode of operation determined by the user inputs. The Start pulse sets GO and calls one of the five programs depending on the mode of operation selected. GO is cleared at the end of all modes except Write or when System Reset is pushed. Write mode ends only when System Reset is generated. The flow chart for the Master (Mode) Control Program is given in Figure 24.

Read Program (Figure 25) is executed when called if Read is set and the Read operation has not been completed. The tape is moved forward, and if the File option is enabled then Search Program is called. Read Mode is set and the file read after the File Name is found. If the File option is not enabled then the whole tape is read (from Initial Load Point to optical end of tape). At the end of the file/at the optical end of tape, the forward command is disabled. If Verify option is enabled then

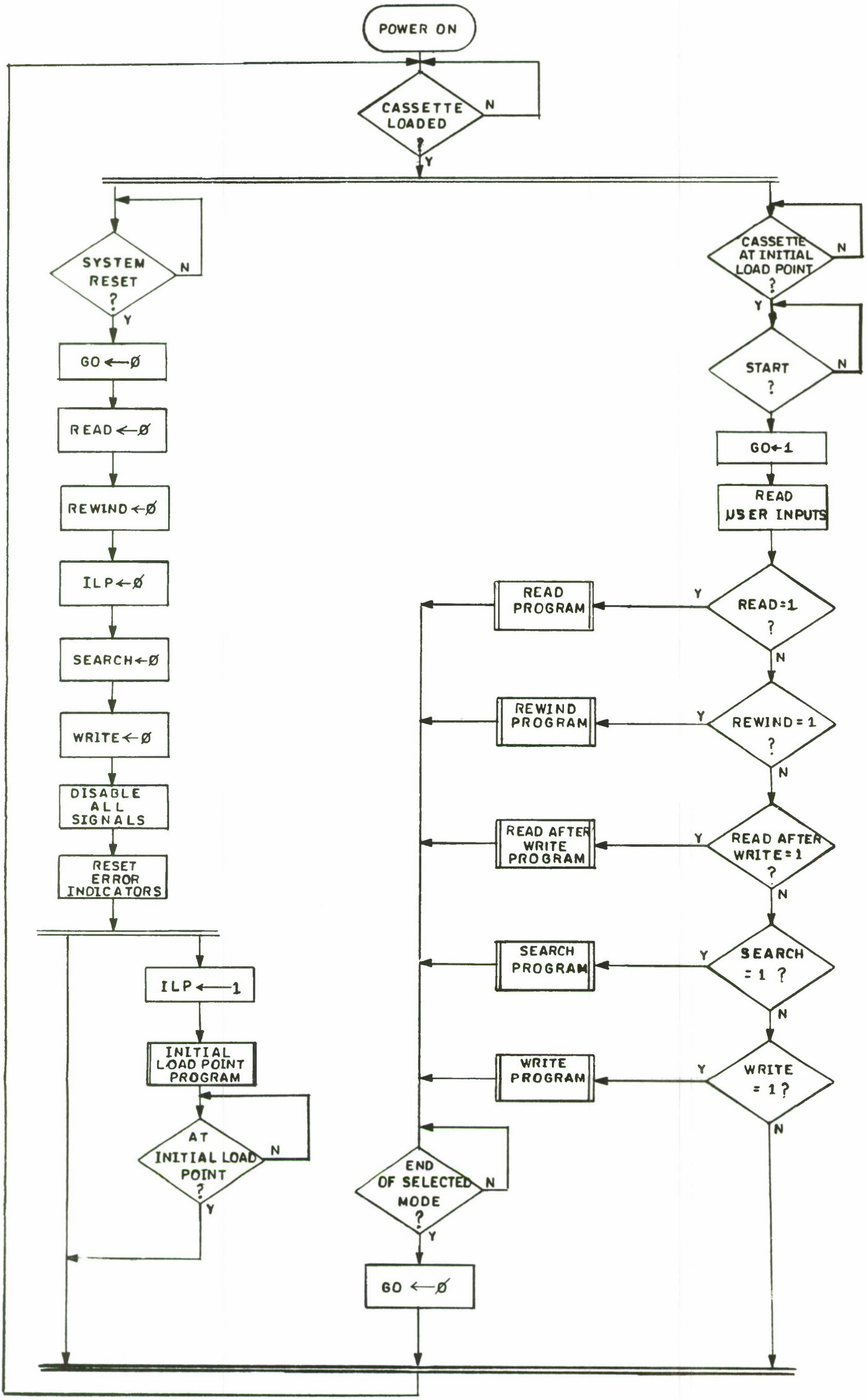


FIGURE 24 MASTER CONTROL PROGRAM

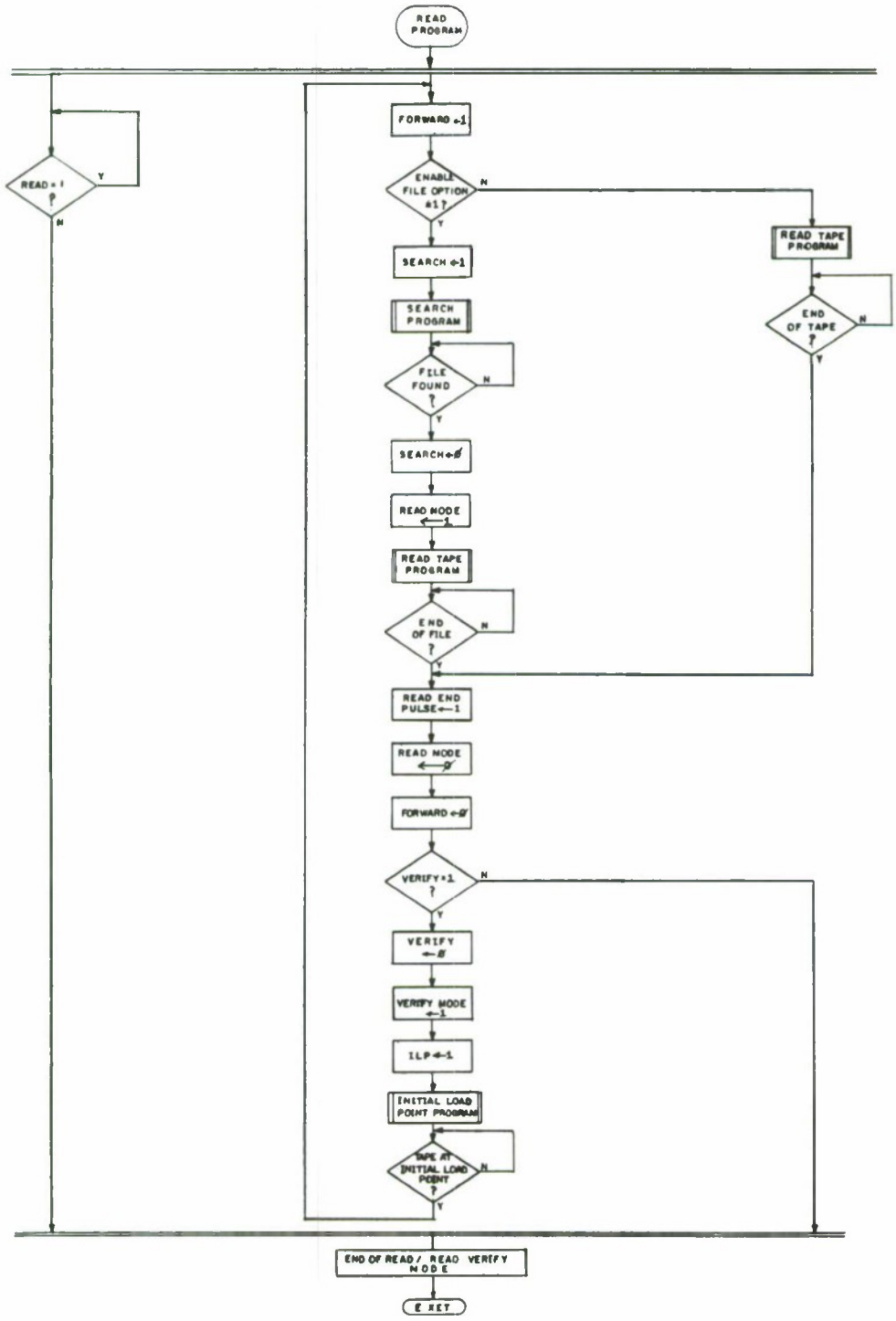


Figure 25 Read Program

the tape is positioned to Initial Load Point and the procedure for Read explained above is repeated. At the end of Read or at the end of Verify if the Verify option is enabled, control is transferred to the Master Control Program.

Read Tape Program (Figure 26) explains the procedure involved in reading a word from the tape. It is executed whenever the tape moves at 10 inches per second in any mode except during Initial Load Point program. In this program three different functions are executed in parallel.

Read File Program (Figure 27) looks for file gap in which no Read Clock is received for 180 milliseconds or more. When the first Read Clock is received at the end of a file gap, the state of the Read File Name is complemented. Every alternate end of a file gap indicates the start of a file name. If the Read File Name goes to the low state at the end of a file gap then it indicates the start of information stored in the file with the name given by the preceding file name. If the file name is not being read and a file gap begins then it indicates the end of a file.

Read Block Program (Figure 28) determines the start and end of blocks. A block end is determined by a lack of Read Clock for more than 2 milliseconds. In Read mode, Output Idle is set after Input Acknowledge for the last word in a block is received.

Read Word Program (Figure 29) reads information off the tape and sends it to an external device if Read Mode is set. At the start of every word the Read Bit Count is reset. The Receive Word Program reads in one bit into one of the two read registers at every Read Clock. When both the registers are full, a check is made to determine if they are equal. If they do not have the same content then the odd parity test is performed and the register that satisfies the odd parity requirement becomes the Out Word. If none of the registers have the correct parity bit then it represents a read error. If both unequal registers have the correct parity bit then a Double Word error is indicated. Register 2 becomes the Out Word if both the registers are equal or both the registers are not equal and either Register 1 does not have the correct parity bit or both the registers have the correct parity bit. If Register 2 is not the Out Word then Register 1 becomes the Out Word. The Out Word is shifted twelve bits to the right if I/O Bits indicates twelve bits per word. A pulse is then generated to indicate that a new Out Word is ready (Out Word Ready Pulse). If the word read is a file name then bit Ø1 of Out Word is stored into I/O Bits (I/O Bit is reset when File Name is read). If word read is not

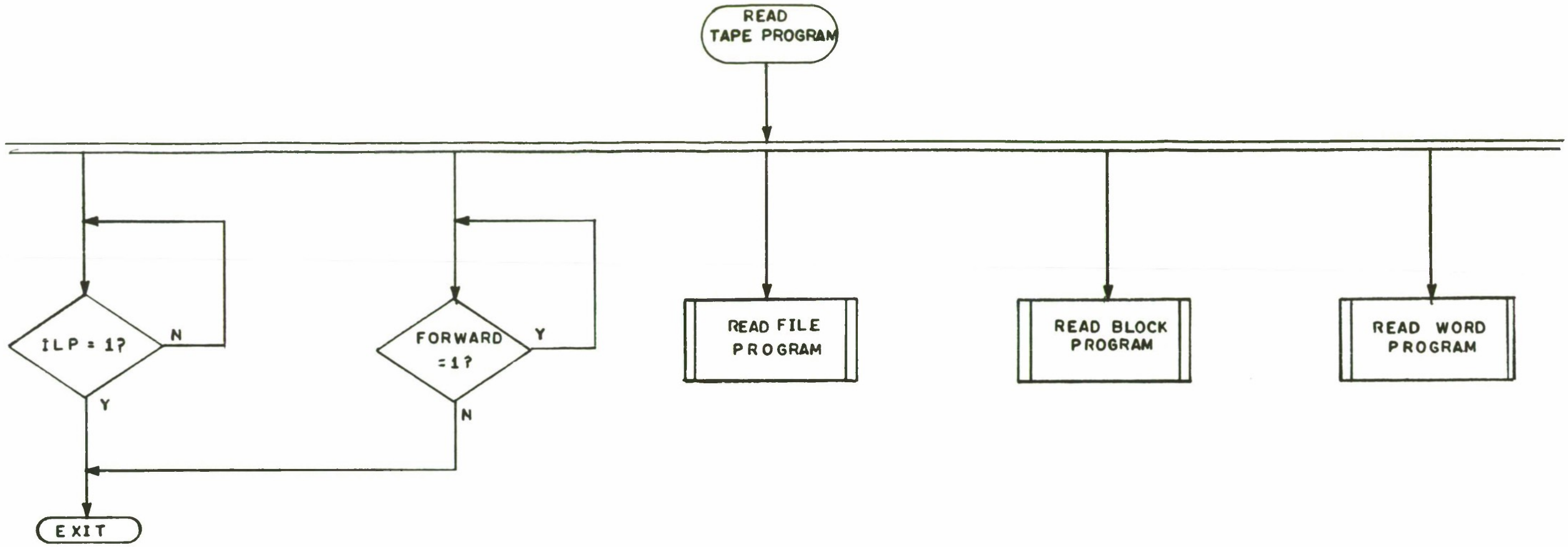


FIGURE 26 READ TAPE PROGRAM

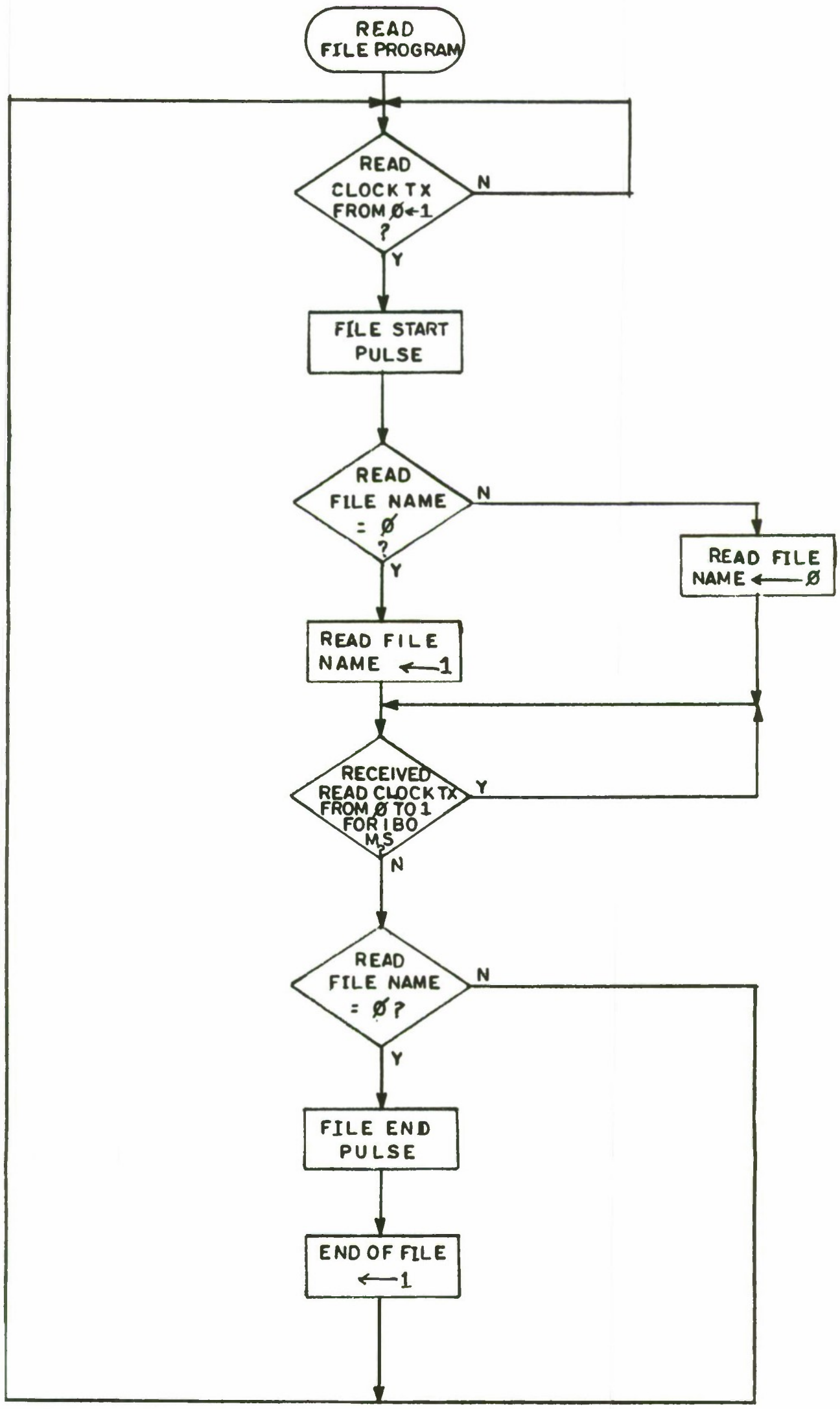


FIGURE 27 READ FILE PROGRAM

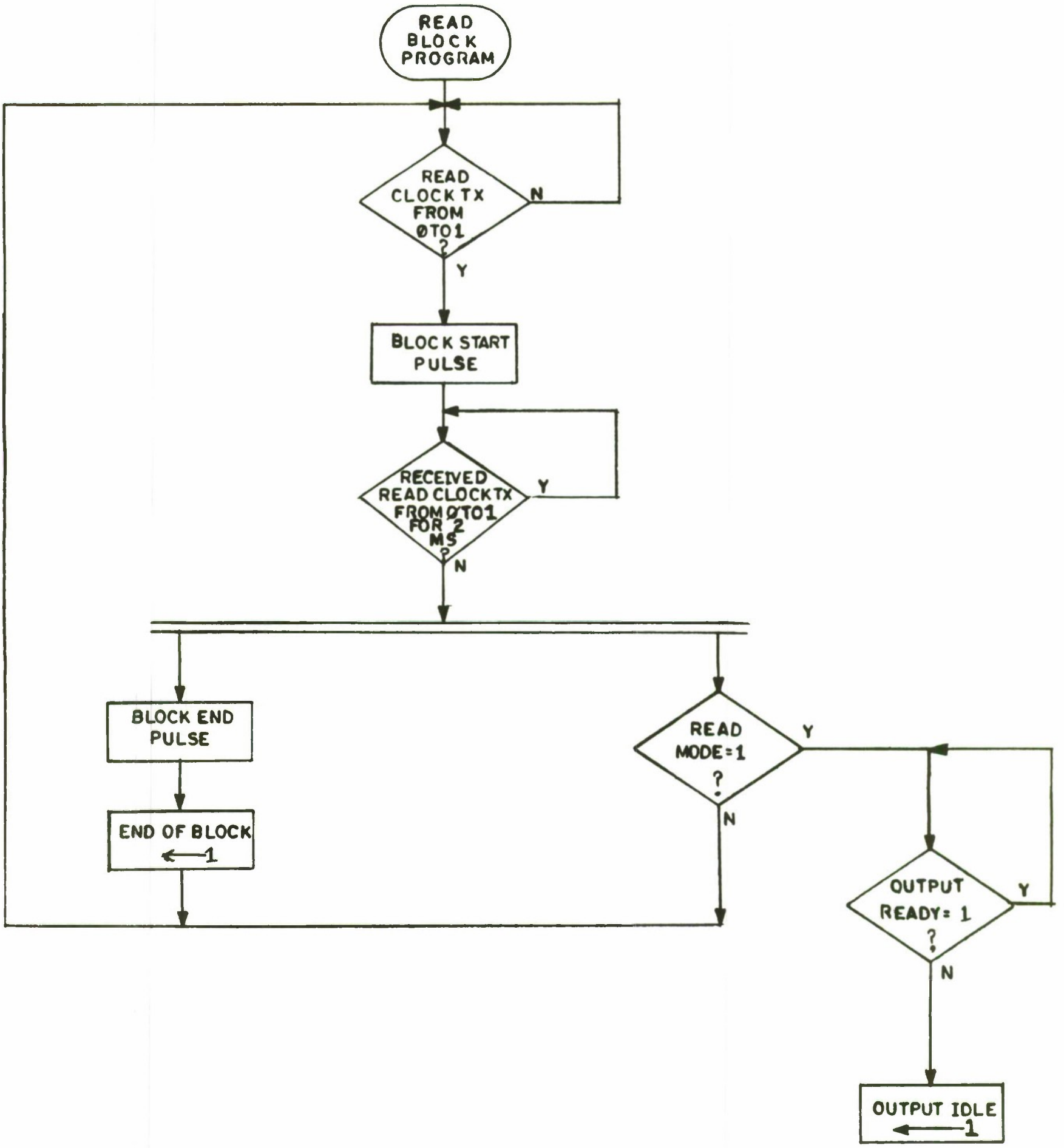


FIGURE 28 READ BLOCK PROGRAM

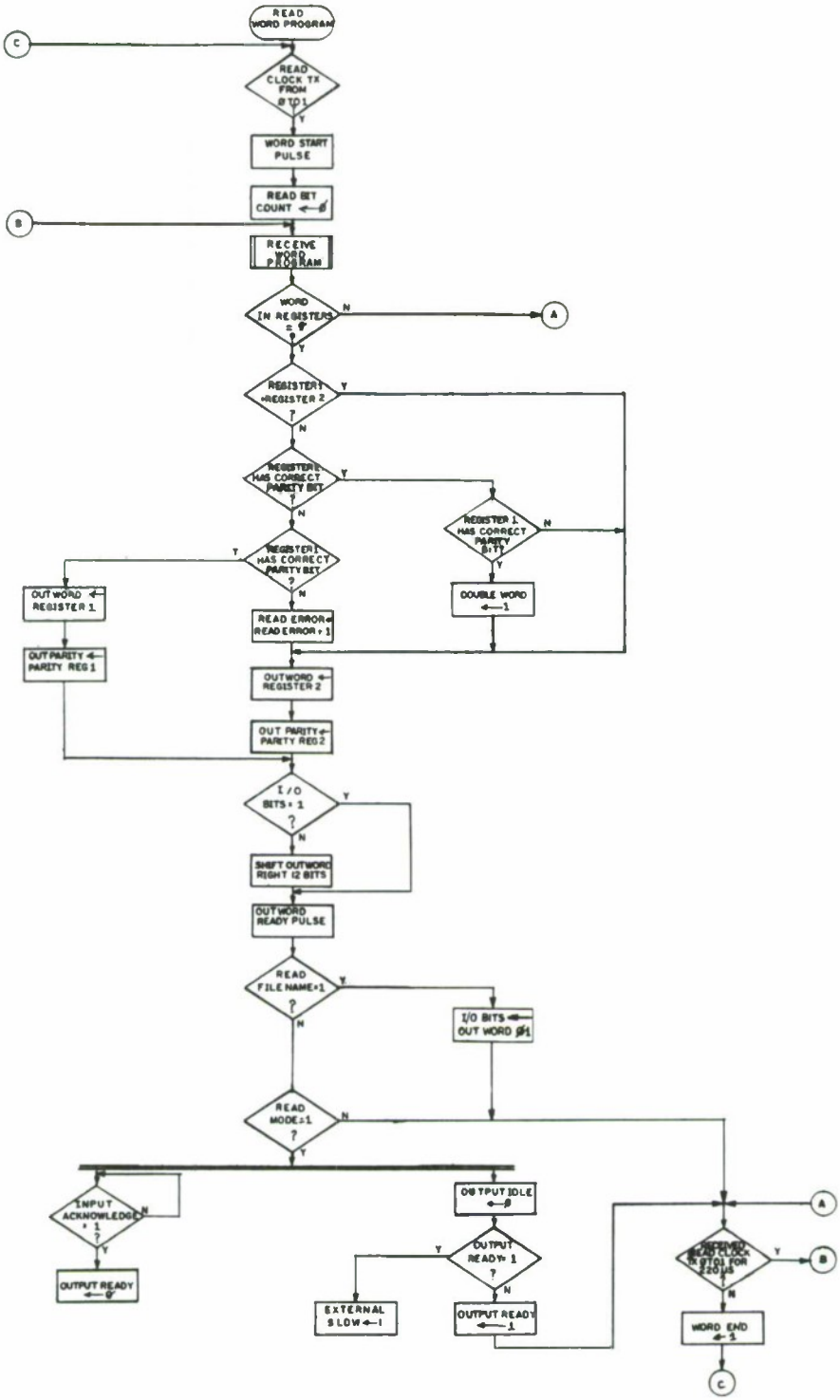


Figure 29 Read Word Program

a file name and Read Mode is set then Output Idle is reset and Output Ready is set. If Output Ready is set when Out Word has a new word then it indicates that the external device is not receiving words at the correct rate. This is an error condition and it is indicated by External Slow. In Read Mode, Output Ready is reset when Input Acknowledge transitions to one. If Read Clock is not received for 220 microseconds then it indicates the end of a word. The Read Word Program then waits for a Ø to 1 transition of Read Clock.

Receive Word Program (Figure 30) reads the Read Data into either Register 1 or Register 2 or Guard Register at every Read Clock. If Read Bit Count is less than two then Read Data is shifted into Guard Register; otherwise, it is shifted into either Register 1 or Register 2. If I/O Bits is 1 (indicating sixteen bits per word)/Ø (indicating twelve bits per word) then the next seventeen/thirteen bits are shifted into one of two read registers and then the Read Bit Count is reset to shift the remaining two bits into Guard Register. At the end of every Read Clock, the Read Bit Count is incremented by one. If both Register 1 and Register 2 are full then Word In Registers is set.

Rewind Program (Figure 31) sets ILP and calls Initial Load Point Program. When the tape reaches the Initial Load Point, control exits from the Rewind Program.

Initial Load Point Program (Figure 32) sets Reverse. The tape moves in the reverse direction until it reaches the physical end. Reverse is then reset and after a pause of 50 milliseconds Forward and Tape Write are enabled causing the tape to be erased while moving in the forward direction until 116 milliseconds after the optical beginning of tape is encountered. Then Forward and Tape Write are disabled and ILP is reset. The end of Initial Load Point Program is indicated, and control is transferred to the calling program.

In Read After Write Program (Figure 33), Write is set and Write Program is called. Read Mode is set if Input Idle is reset and the first input data word has been received. At the end of a file (or block) Read Mode is reset. When Read Mode is set, the words read off the tape after they are written are sent to an external device through the output connector. In this program, all functions are the same as Write Program except that Read Mode is set when a block is being read.

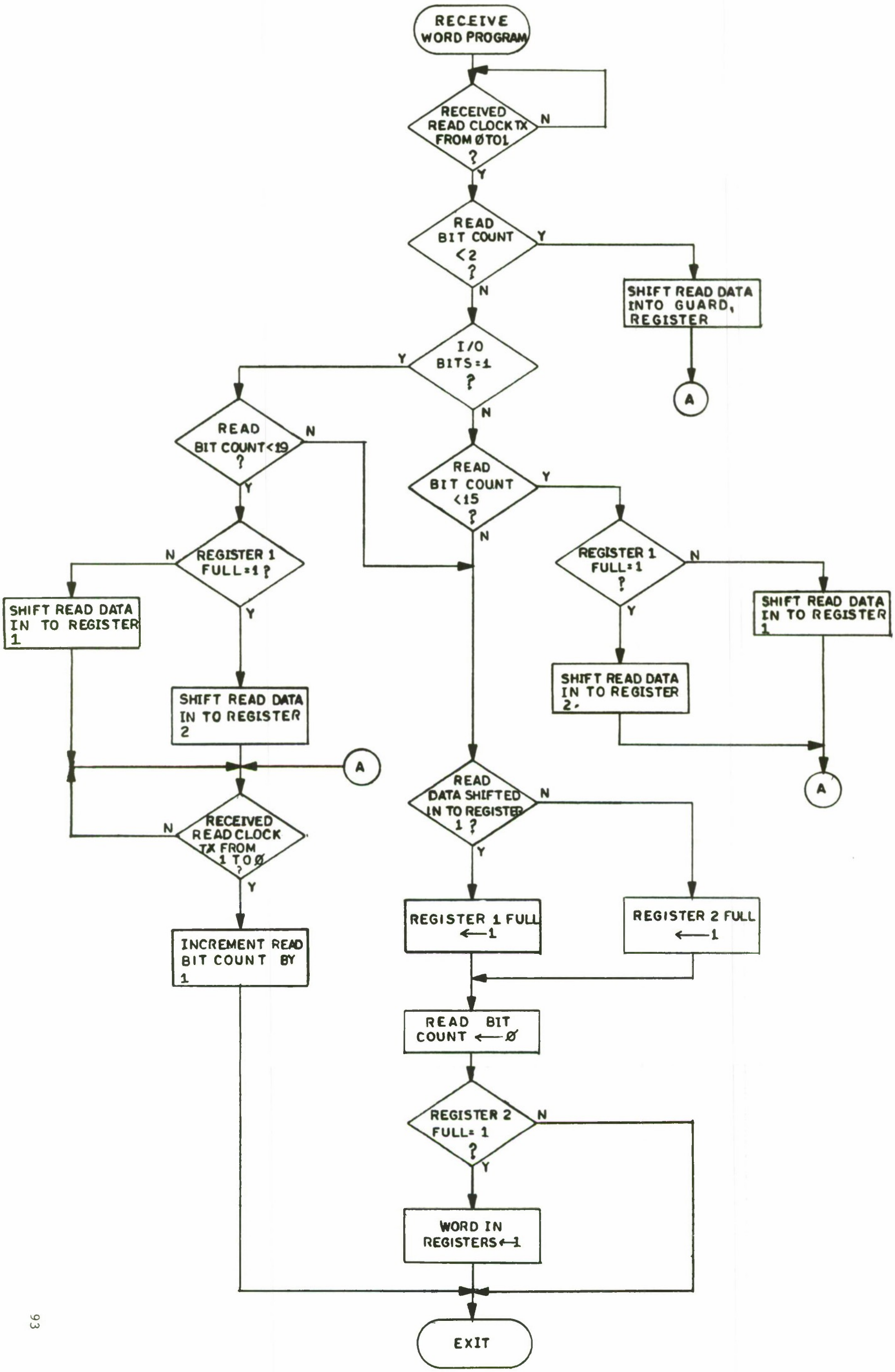


FIGURE 30 RECEIVE WORD PROGRAM

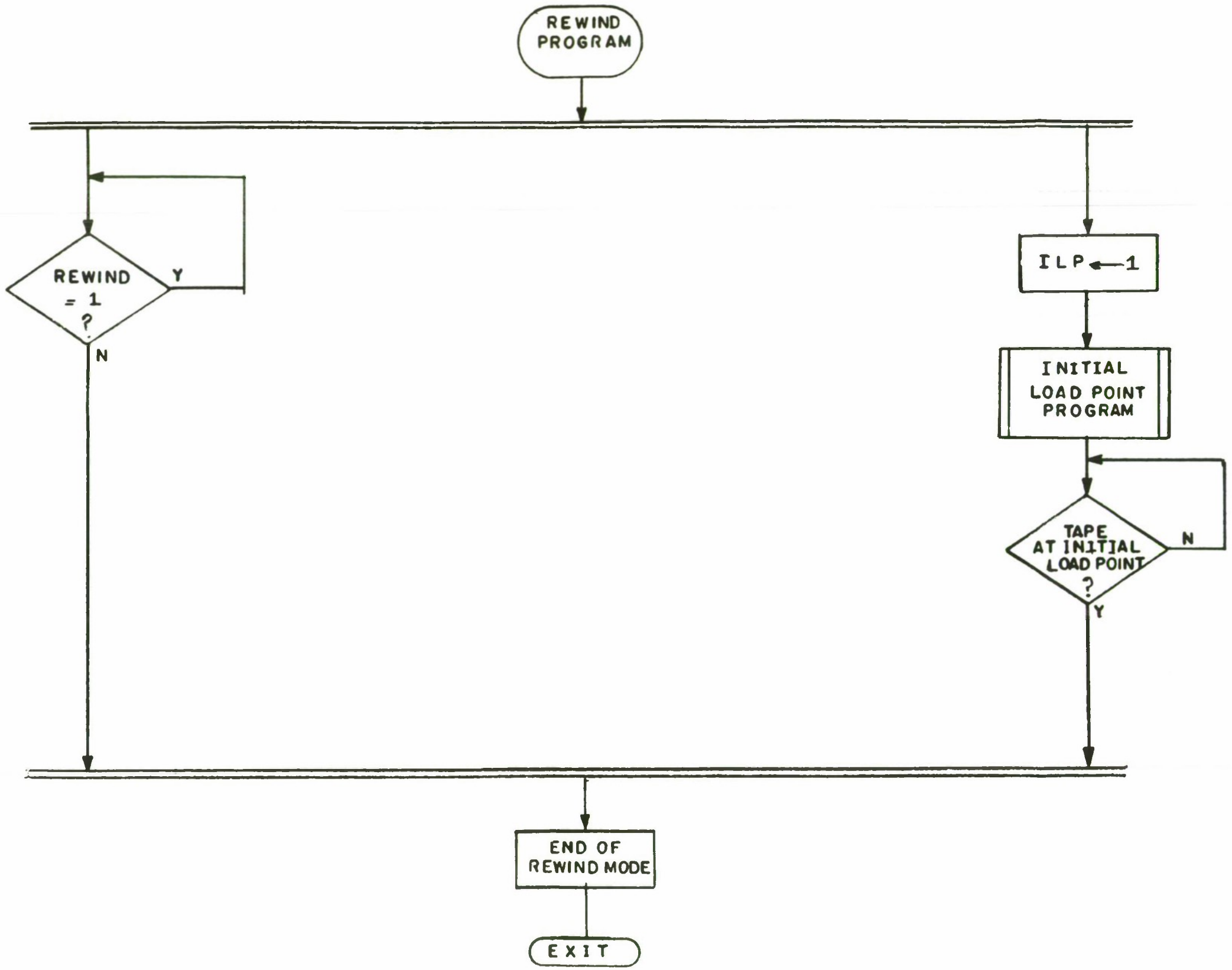


FIGURE 31 REWIND PROGRAM

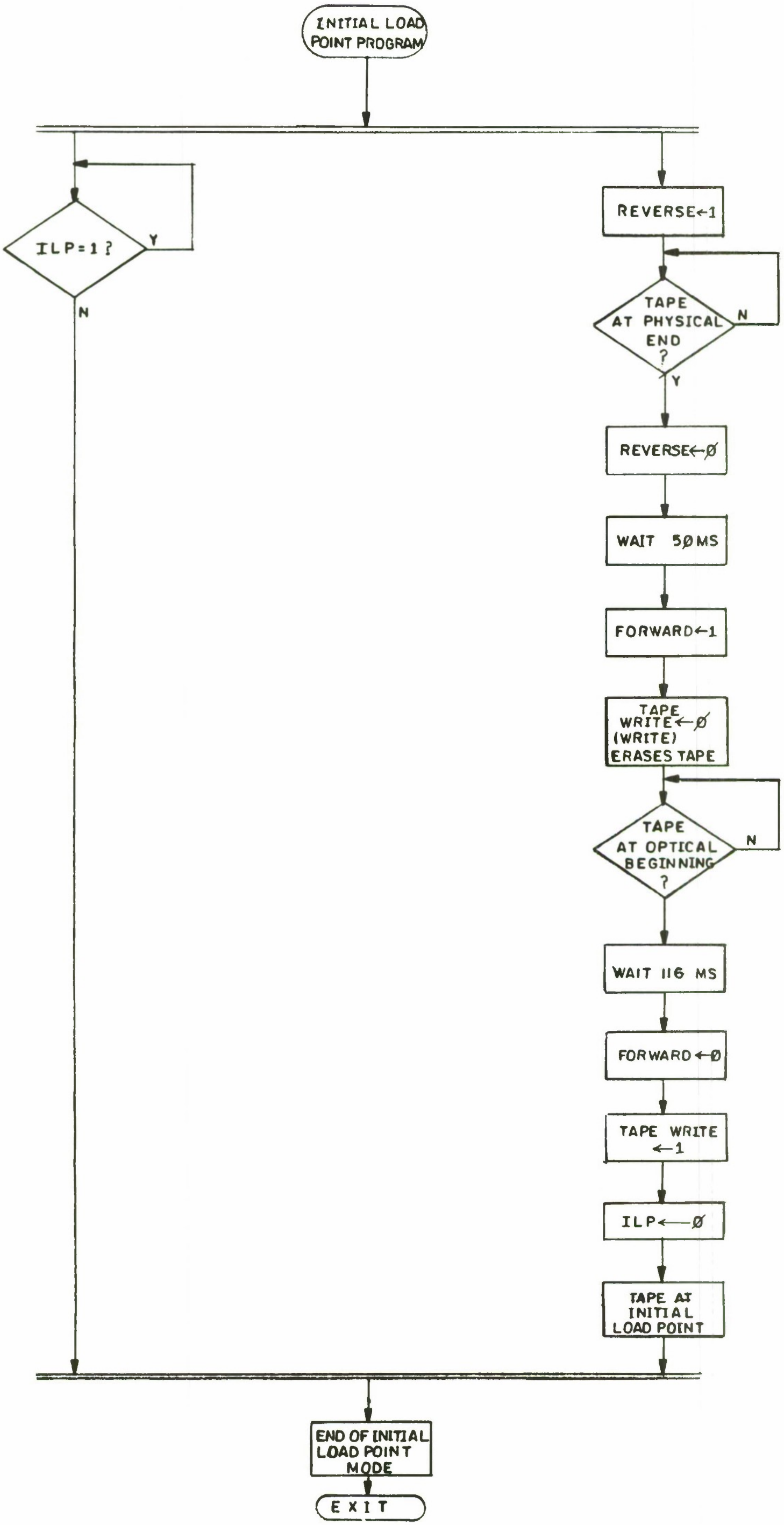


FIGURE 32 INITIAL LOAD POINT PROGRAM

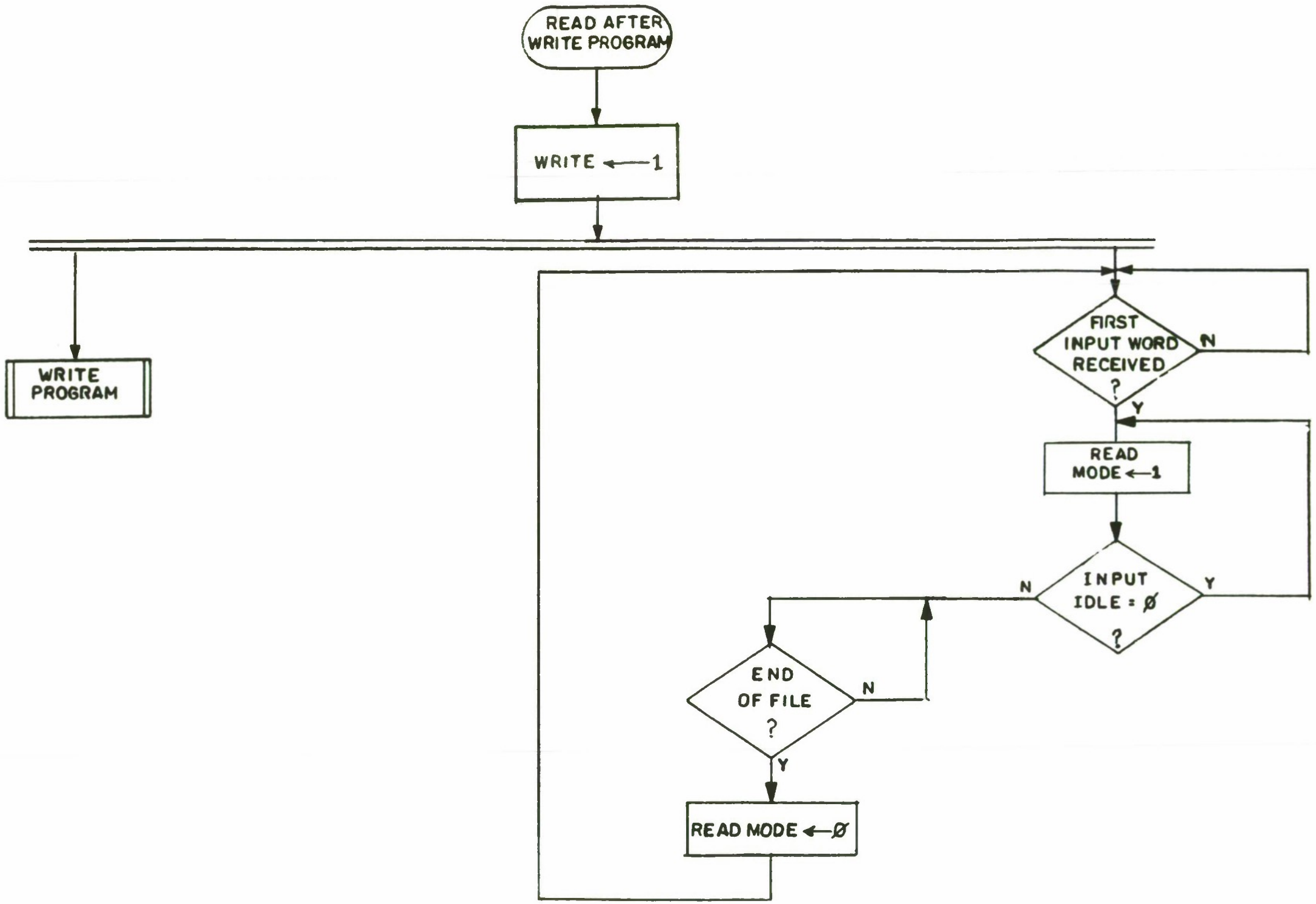


FIGURE 33 READ AFTER WRITE PROGRAM

In Search Program (Figure 34), the tape is moved forward as long as Search is set, file is not found and the tape has not reached the optical end. When the tape moves forward, information is read off the tape by the Read Tape Program. When a file name is read, the least significant ten bits of Out Word are compared with the File Name In. If they are equal, File Found is set and Search is reset. If file is not found and the tape reaches the optical end then File Not Found is set and Search is reset. Whenever Search is reset, control exits from the Search Program.

Write Program (Figure 35) is executed if Write is set. On entering Write Program, Next File Start program is called if Next File Start is set. When the tape is at the next available file start and Write Permit is set then Write Mode and Tape Write are enabled and Write File Program is called. If Write is reset then Tape Write, Forward and Write Mode are disabled and control exits from the Write Program.

When Next File Start Program (Figure 36) is called, the tape should be at the Initial Load Point. Forward is enabled and if Read Clock is not received for 315 milliseconds then it indicates that the tape is empty. Forward is reset, ILP is set, and the Initial Load Point Program is called. When the tape reaches the Initial Load Point, Tape At Next File Start is set and control exits from the Next File Start Program. If the cassette is not empty then the tape is moved forward until no Read Clock is received for at least 315 milliseconds. This indicates the end of information recorded on the tape. If the end of recorded information is not reached before the optical end of tape then Cassette Full is set, Forward is reset and control returns to the calling program. When Cassette Full is set, it indicates that no space is available on the tape to record any new information. When the tape reaches the end of recorded information (at the end of previously recorded data but before end of tape), Forward is reset. After 100 milliseconds, the tape is moved in the reverse direction for 315 milliseconds. At the end of reverse motion, the unit waits for 100 milliseconds and then the Tape At Next File Start is set and control is transferred to the calling program.

Write File Program (Figure 37) is executed when called if Write Mode is set. When Input Idle transition from 1 to Ø is received and Input Ready is set for the first word of the file, then Generate File Name Program is called. After the File Name is written on the tape, four different processes are performed

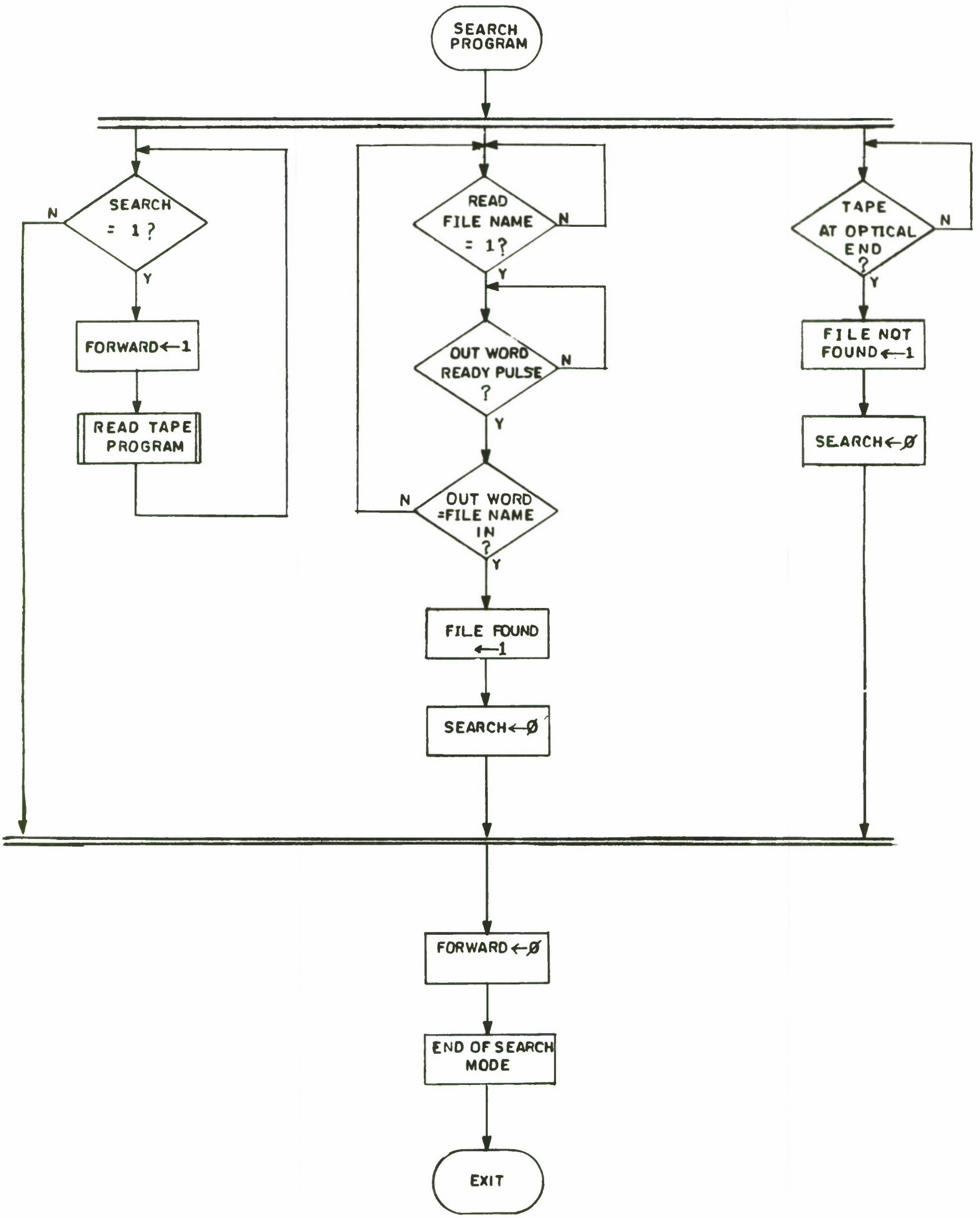


FIGURE 34 SEARCH PROGRAM

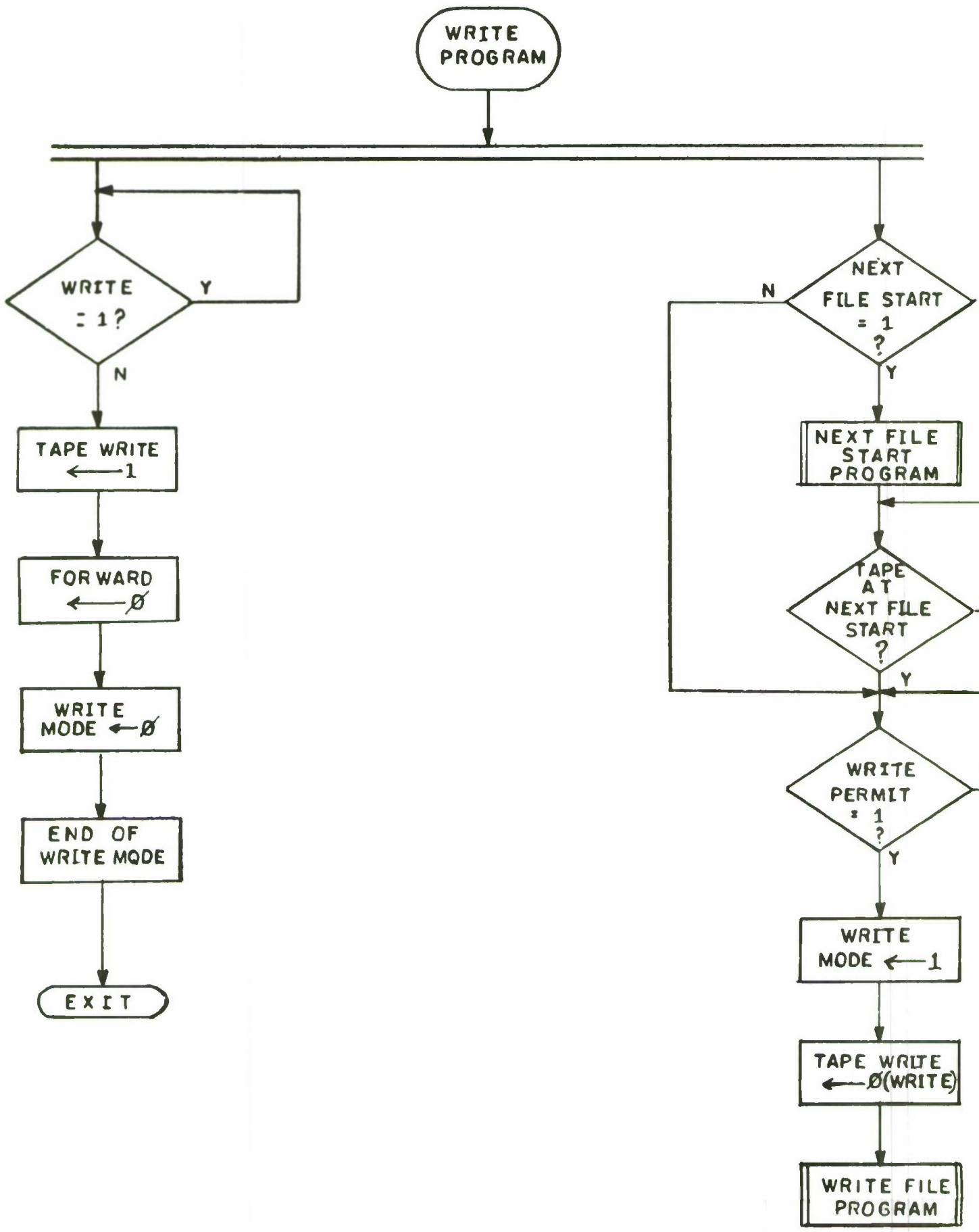


FIGURE 35 WRITE PROGRAM

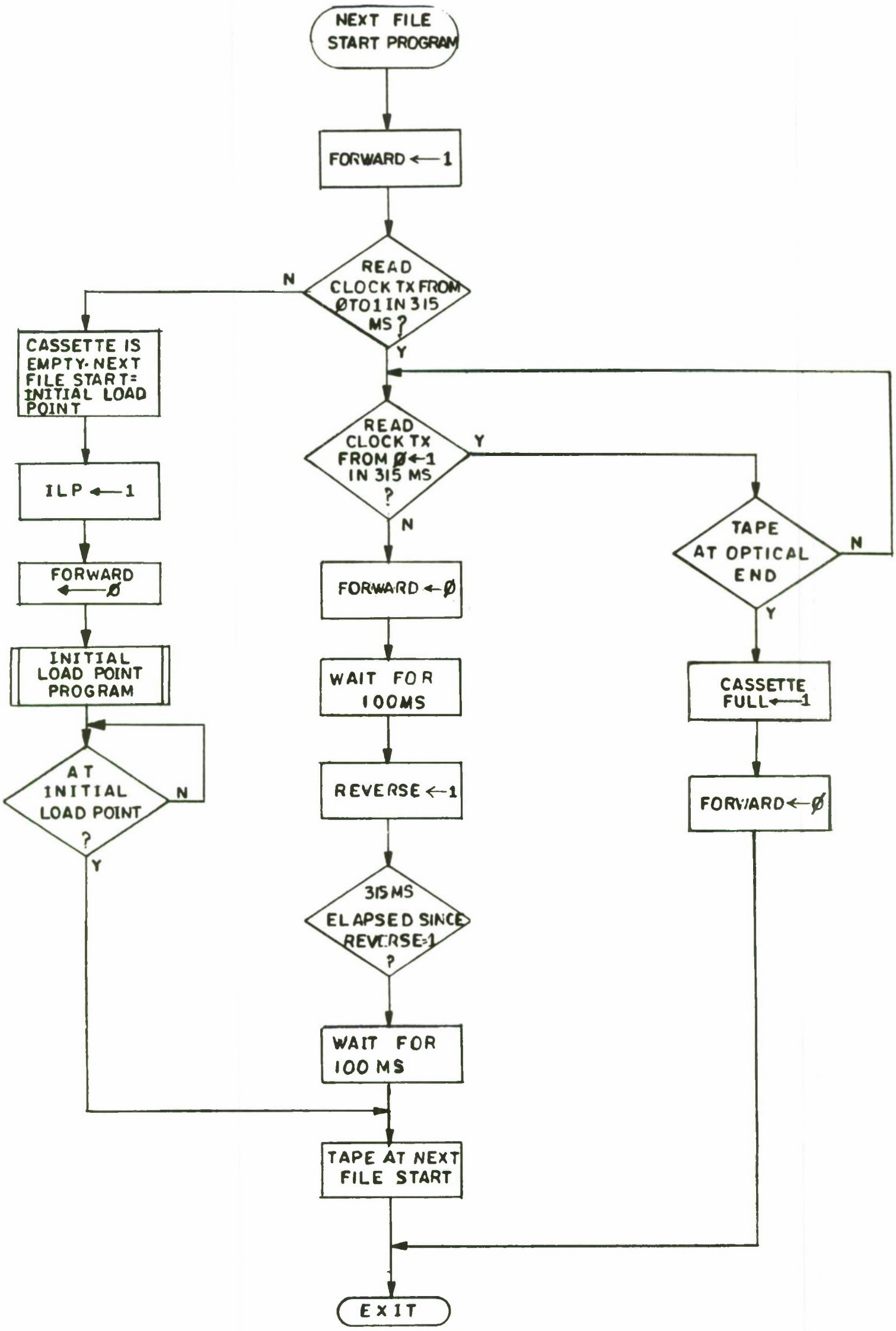


FIGURE36 NEXT FILE START PROGRAM

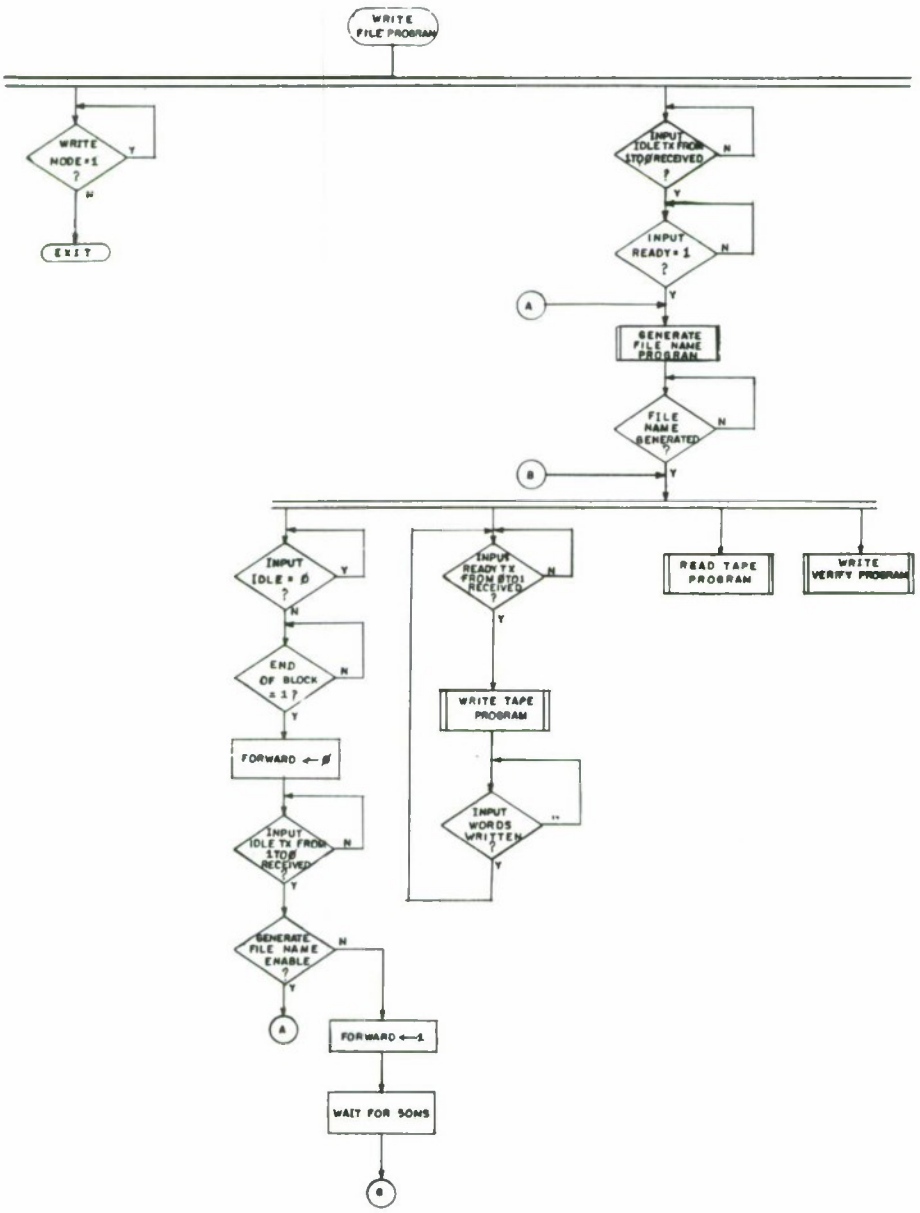


Figure 37 Write File Program

in parallel. First, for every Ø to 1 transition of Input Ready the Input Word is written on the tape by Write Tape Program. Second, the Read Tape Program is called to read back the written words. Third, Write Verify Program is called to compare the words read off the tape with the words written. Fourth, if the Input Idle transitions from Ø to 1 (indicating end of input message) and End of Block is set then Forward is reset. The unit then waits for the next block before it resumes writing. If Input Idle transitions from 1 to Ø and Input Ready is set for the first word then it indicates the start of the next block. If Generate File Name is enabled then Generate File Name Program is called; otherwise, Forward is set and after 50 milliseconds the writing of a block begins. The Write File Program is executed as long as Write Mode is set.

Generate File Name Program (Figure 38) records a file gap, File Name and a second file gap at the start of every file. When called, I/O Bits is reset (File Name is always twelve bits), Forward and Write Enable are set. The tape moves ahead for about 200 milliseconds before four different processes are executed. First, Write Tape Program is called to write the input word onto the tape. After the word is written, the unit waits for 200 milliseconds and then sets Write Enable and File Name Generated before transferring control to the calling program. Second, Write Enable is reset after the input word has been accepted. Third, the Read Tape Program is called to read the file name written and to set I/O Bits to its appropriate value. Write Verify Program is called to compare the file name read to the file name written for errors.

Write Tape Program (Figure 39) records input words onto the tape as long as at least one word is ready to be recorded. Words received from an external device are stored in one of two registers. When one of these two registers is ready with an input word, the word stored in that register is recorded onto the tape. If at least one of Otregl and Otreg2 is ready with a word to be recorded and Write Enable is set then Write Clock is generated. If Write Enable is set and Input Ready has transitioned from Ø to 1 then Input Word Accepted is reset. The input word is read into Otregl if Otregl is ready for input; otherwise, it is read into Otreg2 if Otreg2 is ready for input. If none of them is ready for input then it waits until at least one of Otregl Input Ready or Otreg2 Input Ready is set. After the input word is read into a register, the Input Ready for that register is reset and the corresponding Output Ready is set. Input Word Accepted and Output Acknowledge are set. Output Acknowledge is reset after Input

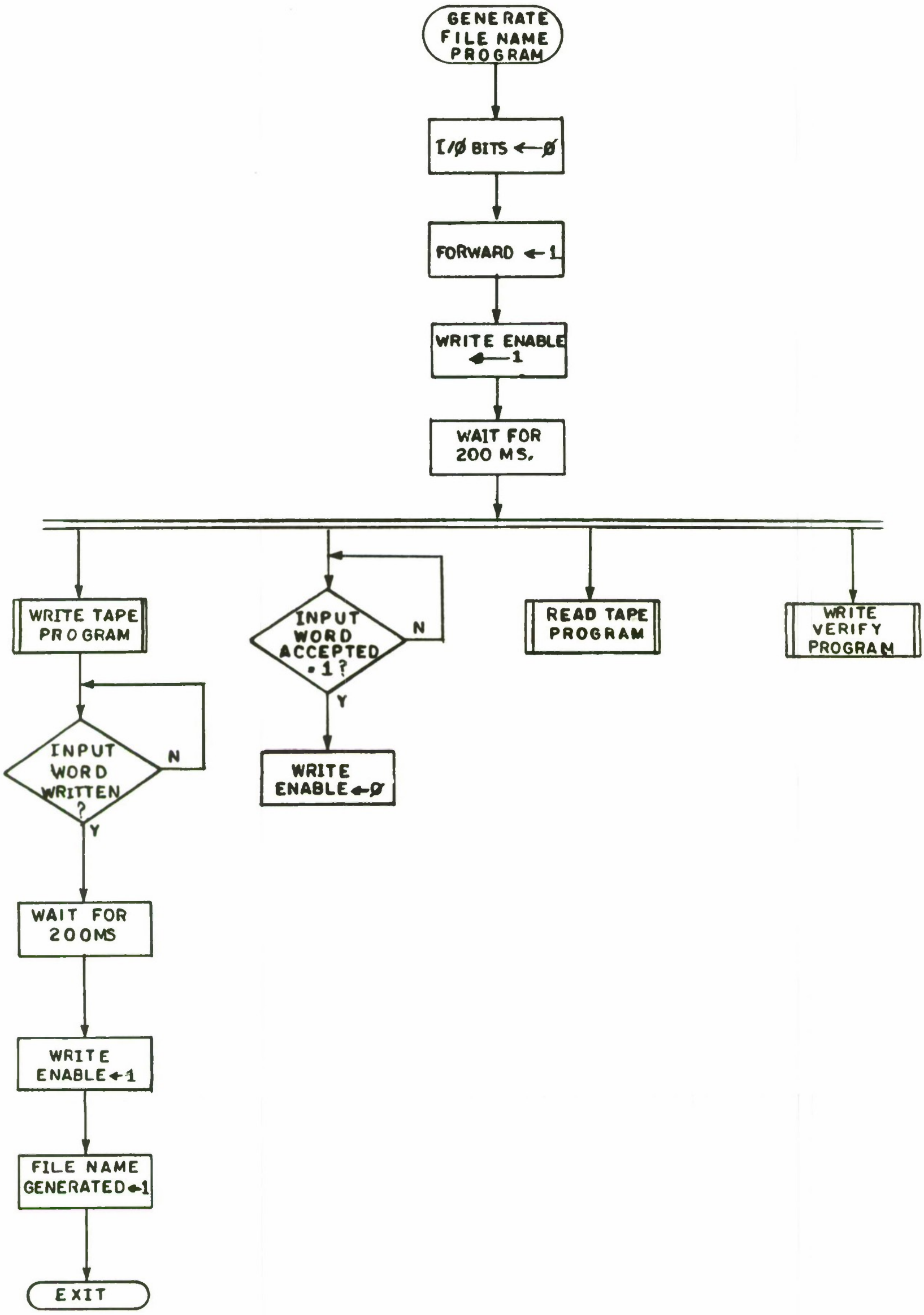


FIGURE 38 GENERATE FILE NAME PROGRAM

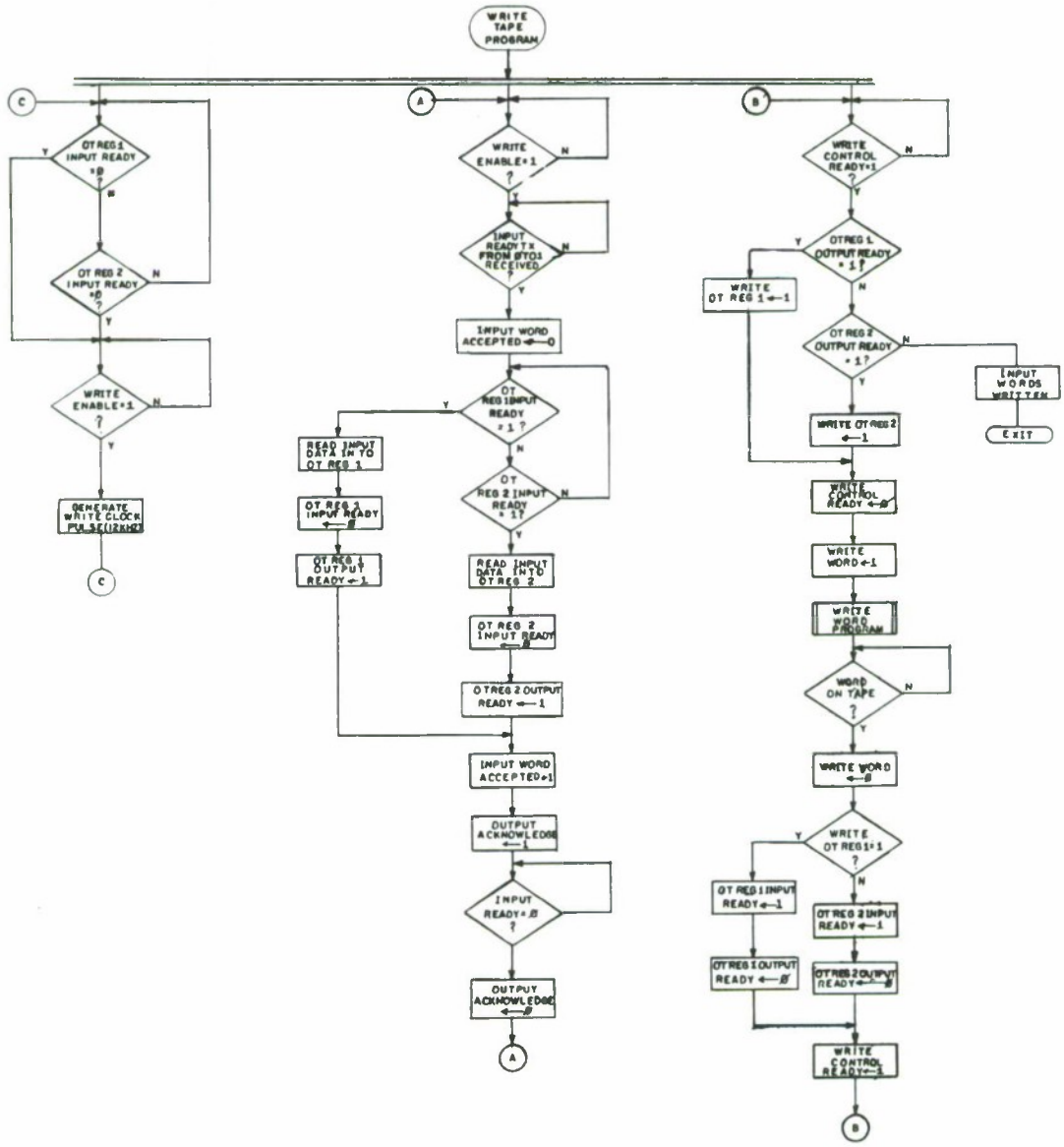


Figure 39 Write Tape Program

Ready transitions to Ø. If Write Control Ready is set then it indicates that the unit is ready to write a word onto the tape. If Otreg1 Output Ready is set then the word stored in Otreg1 is written; otherwise, if Otreg2 Output Ready is set then the word stored in Otreg2 is written. If both Otreg1 and Otreg2 Output Ready are reset then it indicates that all input words have been written and control exits from the Write Tape Program. If there is a word to be written then Write Control Ready is reset, Write Word is set and Write Word Program is called. After the word is written, Write Word is reset and the Input Ready and Output Ready corresponding to the register from which the word was written are respectively set and reset. Write Control Ready is then set and the next word written if the Output Ready for anyone of Otreg1 or Otreg2 is set.

Write Word Program (Figure 40) records a word onto the tape. The word (twelve/sixteen bits) from the register to be used for the write process is loaded into the Write Shift Register with a two-bit preamble and the odd parity bit for the input word. Record Tape is reset (erase) and the Word Gap Count is incremented at every Write Clock Pulse. When Word Gap Count equals four, it is reset and Record Tape is set (record). At every Write Clock Pulse, the Word Bit Count is incremented by one and the Write Shift Register shifted one bit to the right. When the Word Bit Count reaches a count of 14/18 (for twelve/sixteen bits per word), the two-bit suffix is loaded into the Write Shift Register. When the Word Bit Count reaches a count of 17/21 (for twelve/sixteen bits per word), it indicates the end of recording the input word once. Record Tape and Word Bit Count are reset and Word Record Count is incremented by one. The procedure to record the word for a second time is repeated as explained above. After the word has been recorded twice, Word Recorded On Tape is set and control returns to the calling program.

Write Verify Program (Figure 41) compares the word read and the word written for errors during the write process. It employs a 272-bit storage which is composed of sixteen 17-bit words. It has two four-bit address registers; one is used for input address, and the other is used for output address. It is used as a first-in-first-out buffer. This memory is used for storage of words written. When Write Word is set (it indicates that a word is being written) and Memory Busy is reset, the word to be written with the parity bit is stored at the address given by the Input Address Register. The Input Address Register is then incremented and control exits from this program. When a word has been read

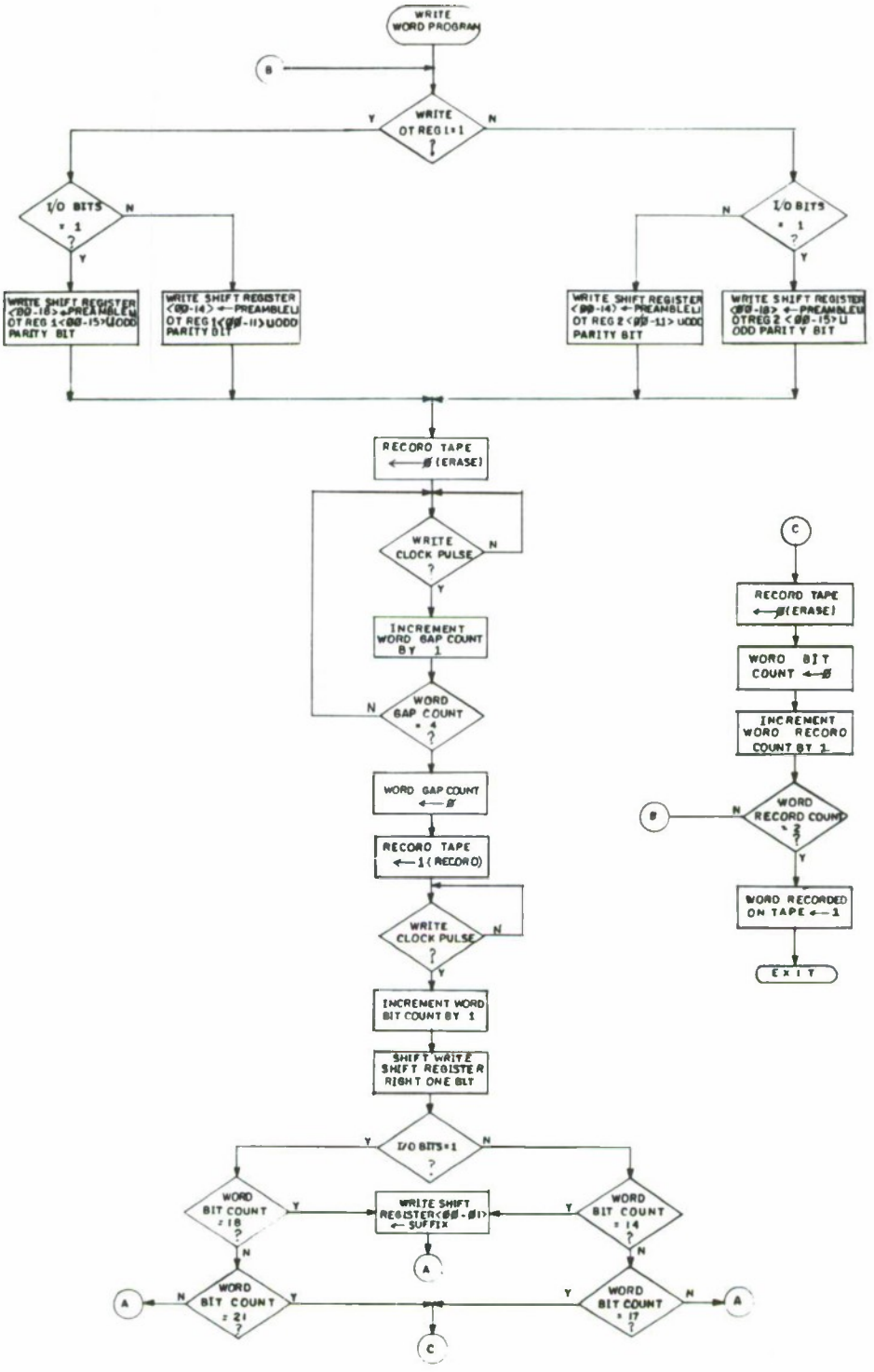


Figure 40 Write Word Program

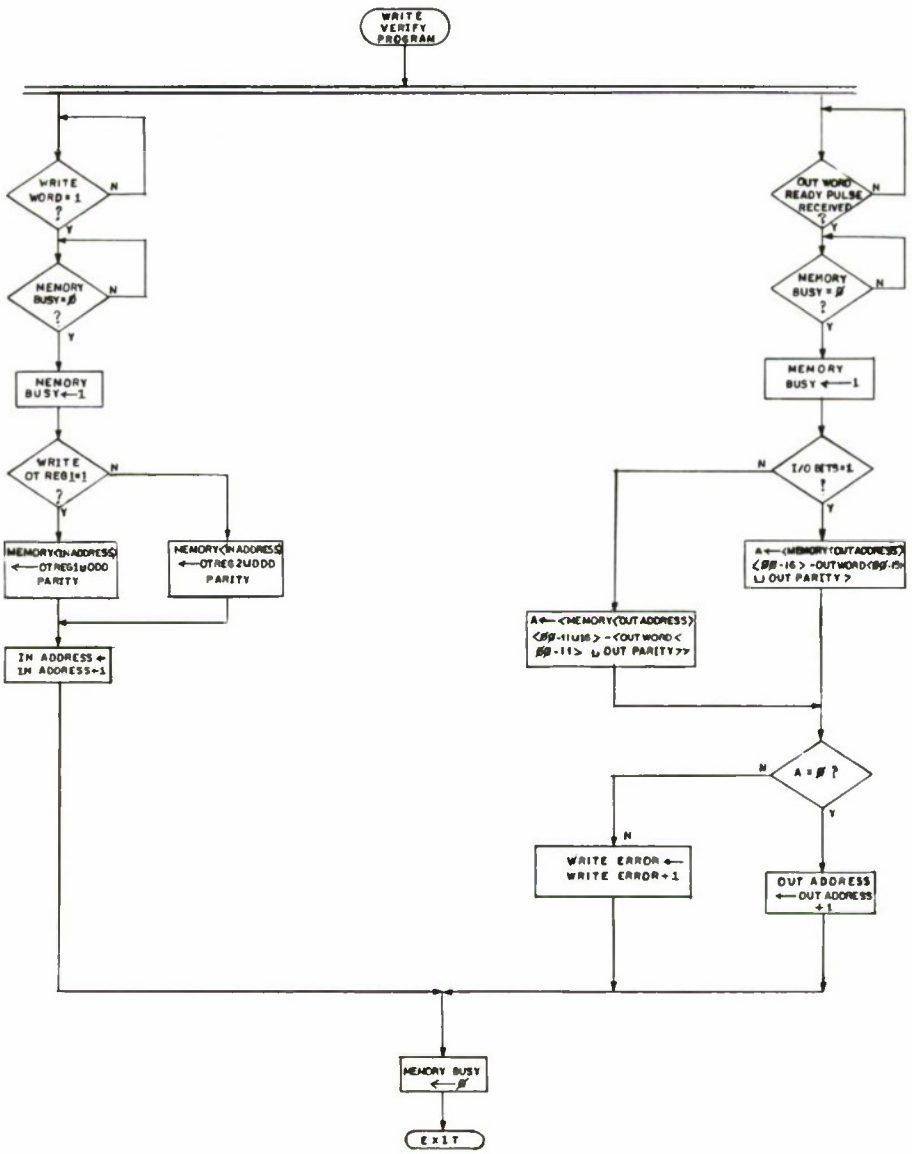


Figure 41 Write Verify Program

and Out Word Ready Pulse is received, the content of the memory at the location given by Output Address Register is compared with twelve/sixteen (depending on the value of I/O Bits) most significant bits of Out Word if Memory Busy is reset. If the comparison indicates unequal quantities then Write Error is incremented by one. One is added to Out Address and control exits from this program.

This completes the description of DACTS hardware. The logic circuit is given in Figures 42 to 62.

AGE Interface can be divided functionally into three sections. These sections may be identified as Master Control, Input Interface and Computer Interface. Each section performs some function during the operation of the AGE Interface in one of its three modes. The hardware description of AGE Interface is divided into three basic sections according to the modes.

When AGE Interface power is turned on, all signals excluding mode and error indicators are reset and Single Instruction Mode and GSE Operational are enabled. System/4Pi CP-2 is forced into single instruction mode and 4π-Storage Busy indicator should be off. If System/4Pi CP-2 power is on and AGE Interface is connected to a 4Pi CP-2 computer then two functions are performed in parallel. If Sysrst pushbutton is pressed then Single Instruction Mode and GSE Operational are disabled. When Sysrst is released, System/4Pi CP-2 is reset and if a program is being executed then 4π-Storage Busy indicator will turn on. System/4Pi CP-2 will continue to execute the program if Single Instruction Mode is disabled and executable information exists in its memory. If Start is pushed then it acts as a system clear in the "pushed" position and resets all signals except error indicators. If clock pulse CP1 is received from System/4Pi CP-2 after Start is released then the user inputs are read and AGE Interface goes to the appropriate mode. If Load Input is set then Load Program is called. At the end of Load Program GO is reset if Verify Read File input transitions from Ø to 1. Then or if Load Input is reset and Verify Input is set initially then Verify Program is called. After all the functions for the mode selected are performed, AGE Interface waits until start is pushed again. This control program is shown in Figure 63.

In Load Program (Figure 64), Load Mode is set, Verify Mode is reset and File In Program is called. Control returns to the calling program when file ends or an error in control bits is detected.

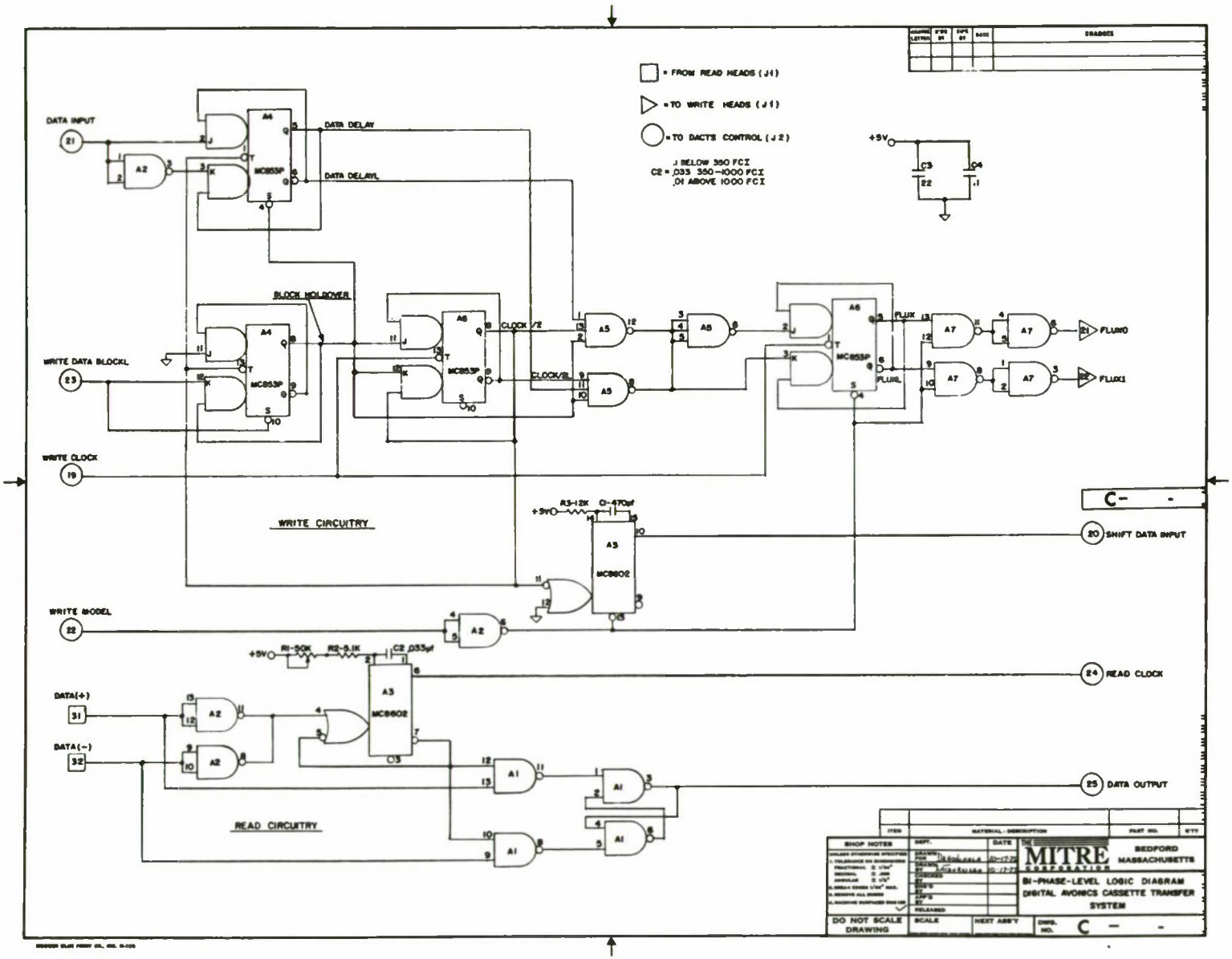


Figure 42 Bi-Phase-Level Logic Diagram Digital Avionics Cassette Transfer System

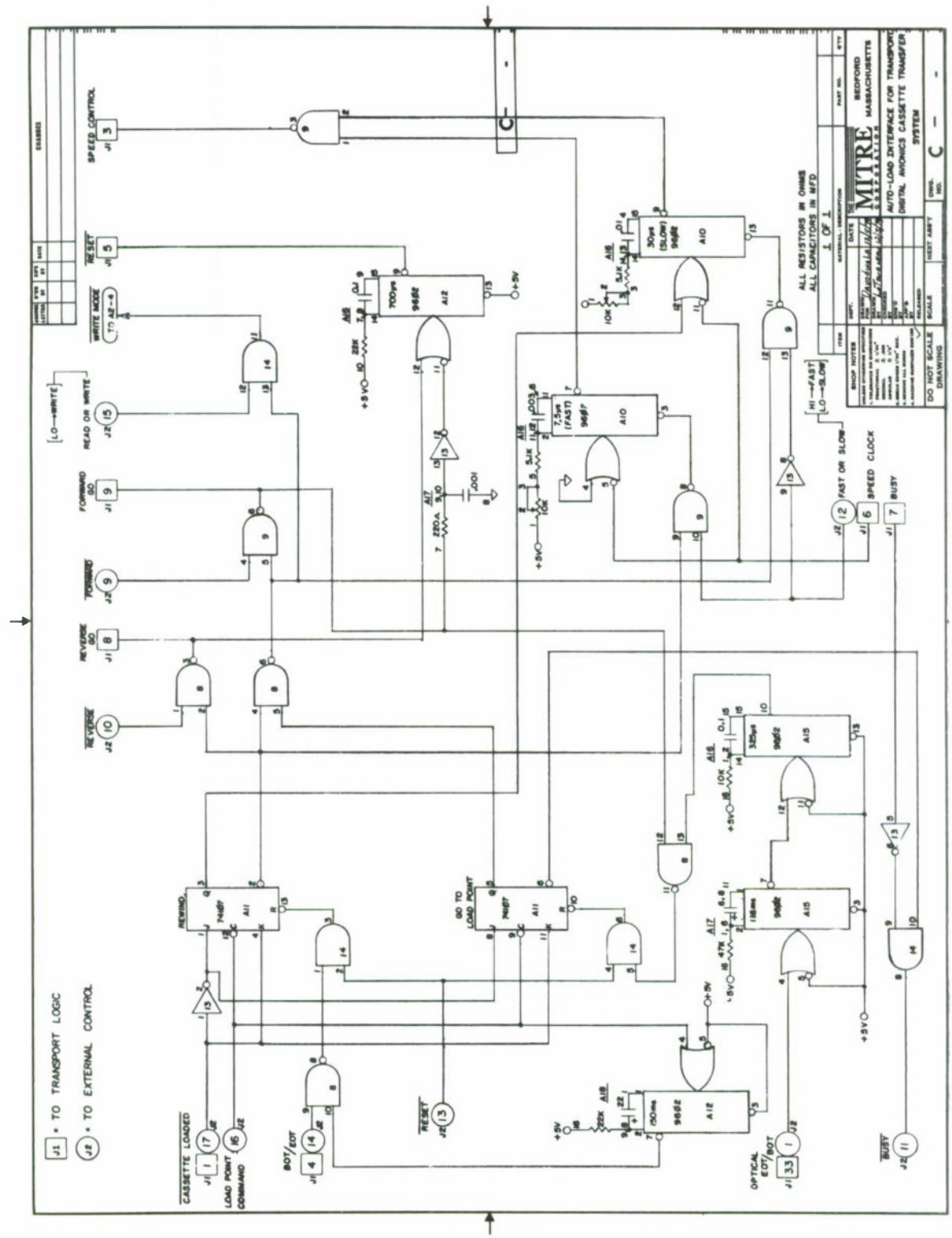


Figure 43 Auto-Load Interface for Transport Digital Avionics Cassette Transfer System

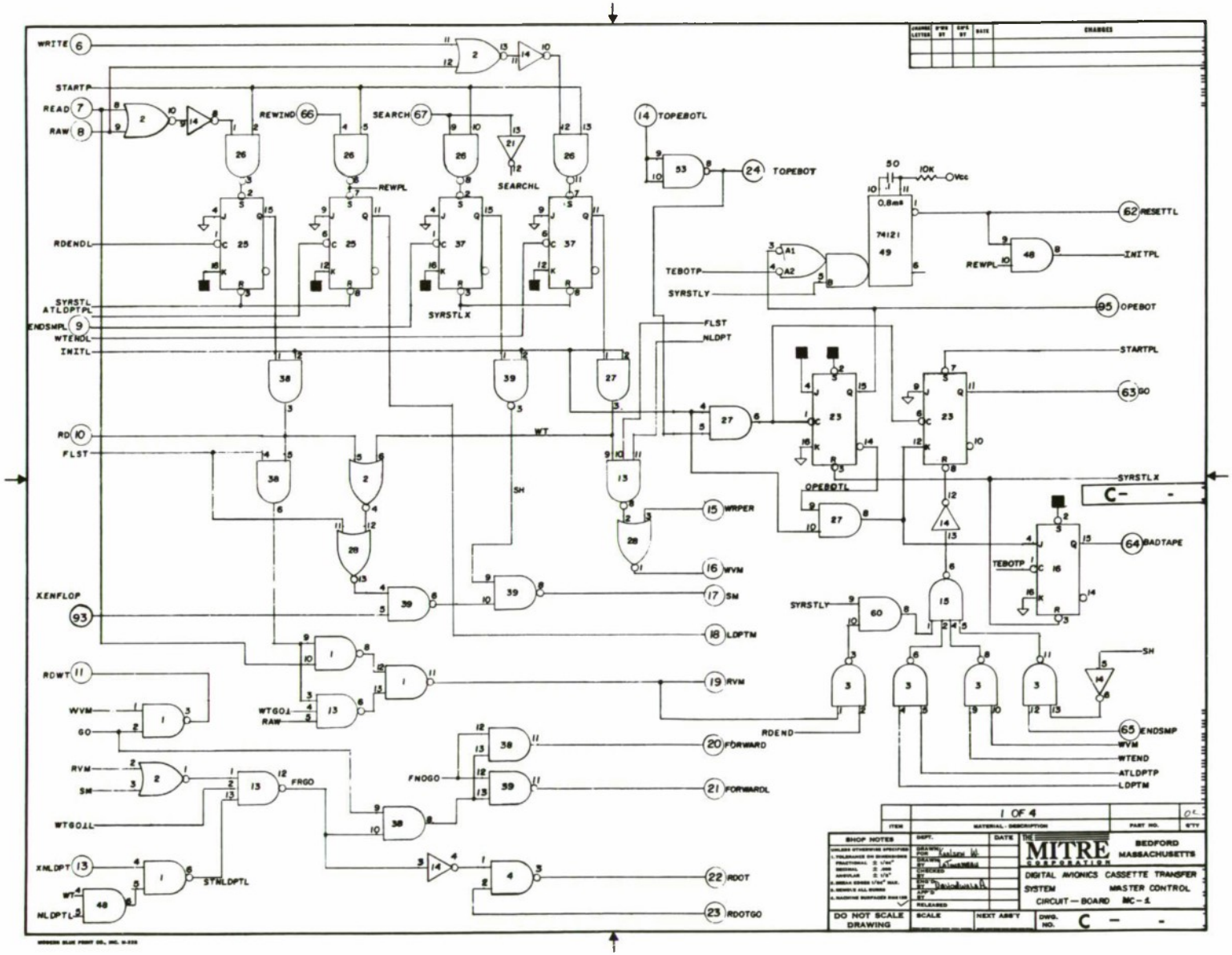


Figure 44 Digital Avionics Cassette Transfer System Master Control Circuit - Board MC-1

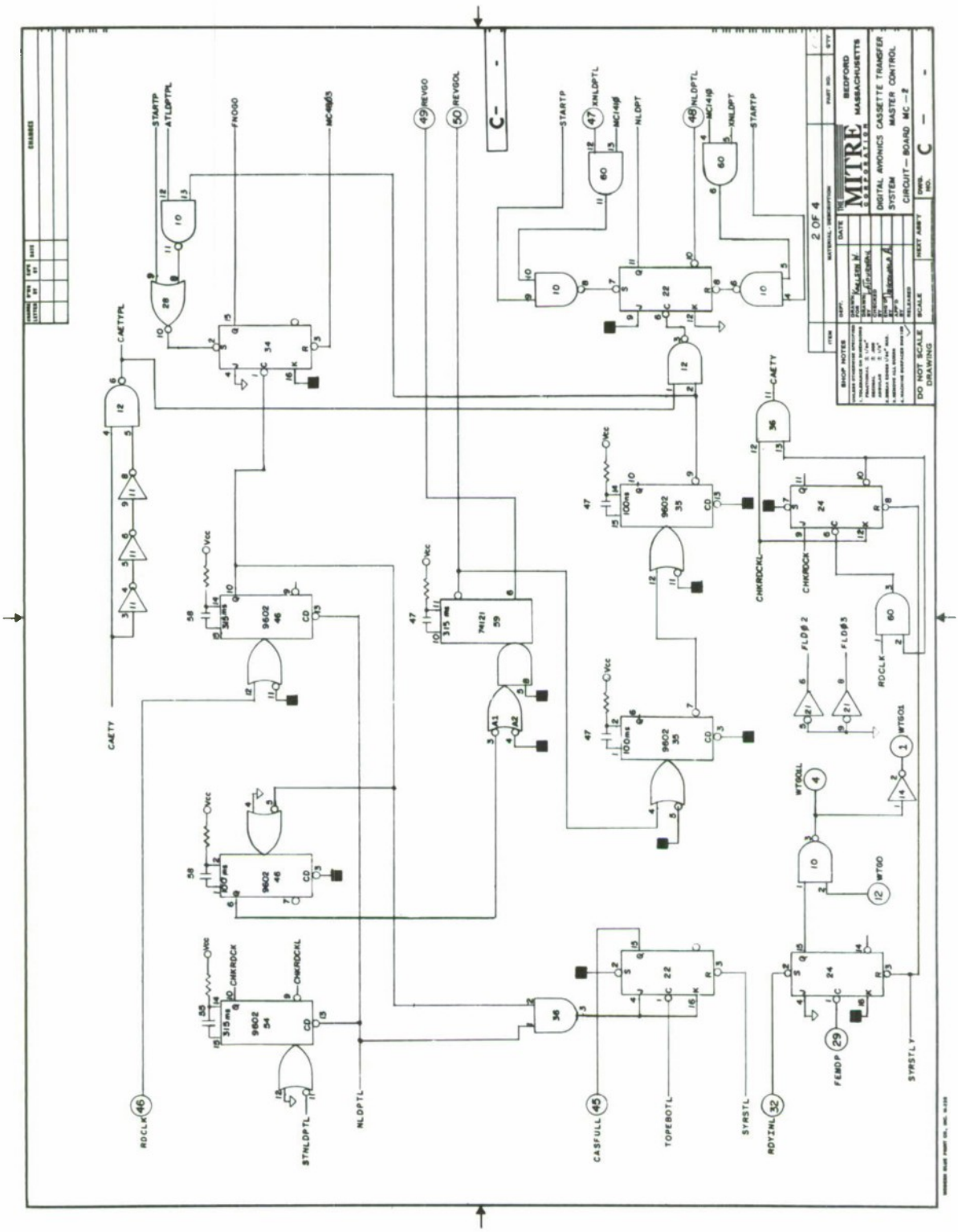


Figure 45 Digital Avionics Cassette Transfer System Master Control Circuit - Board MC-2

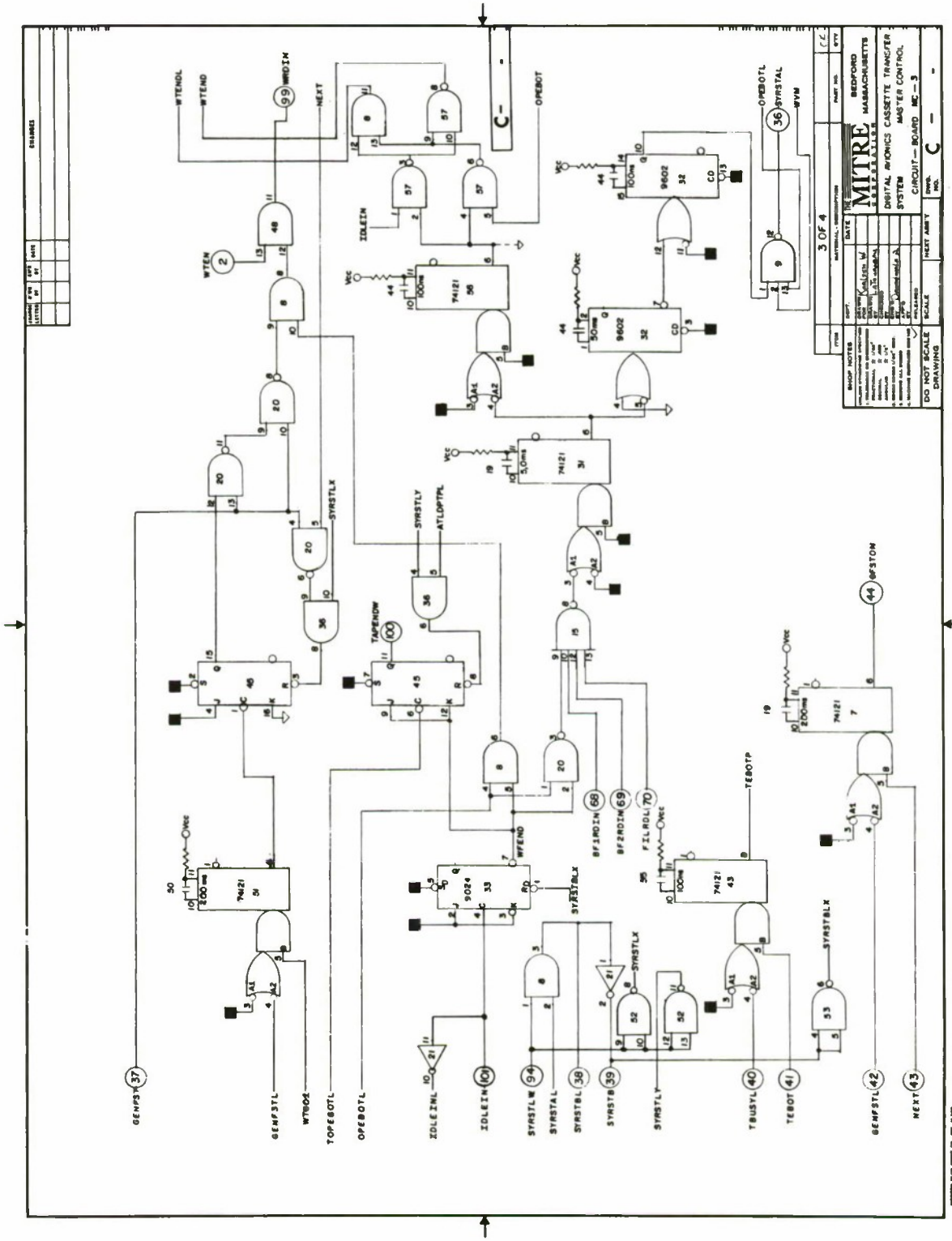


Figure 46 Digital Avionics Cassette Transfer System Master Control Circuit - Board MC-3

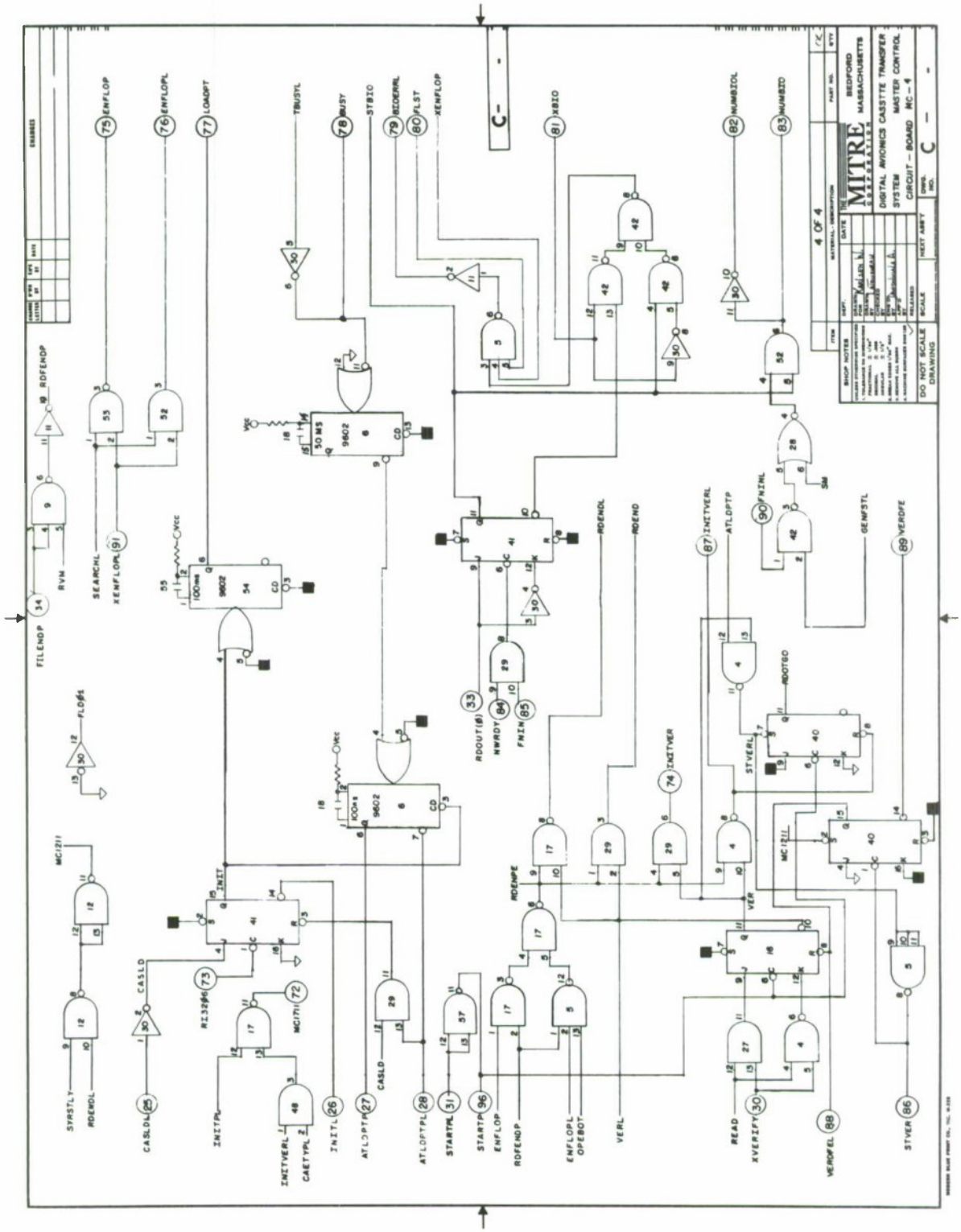


Figure 47 Digital Avionics Cassette Transfer System Master Control Circuit - Board MC-4

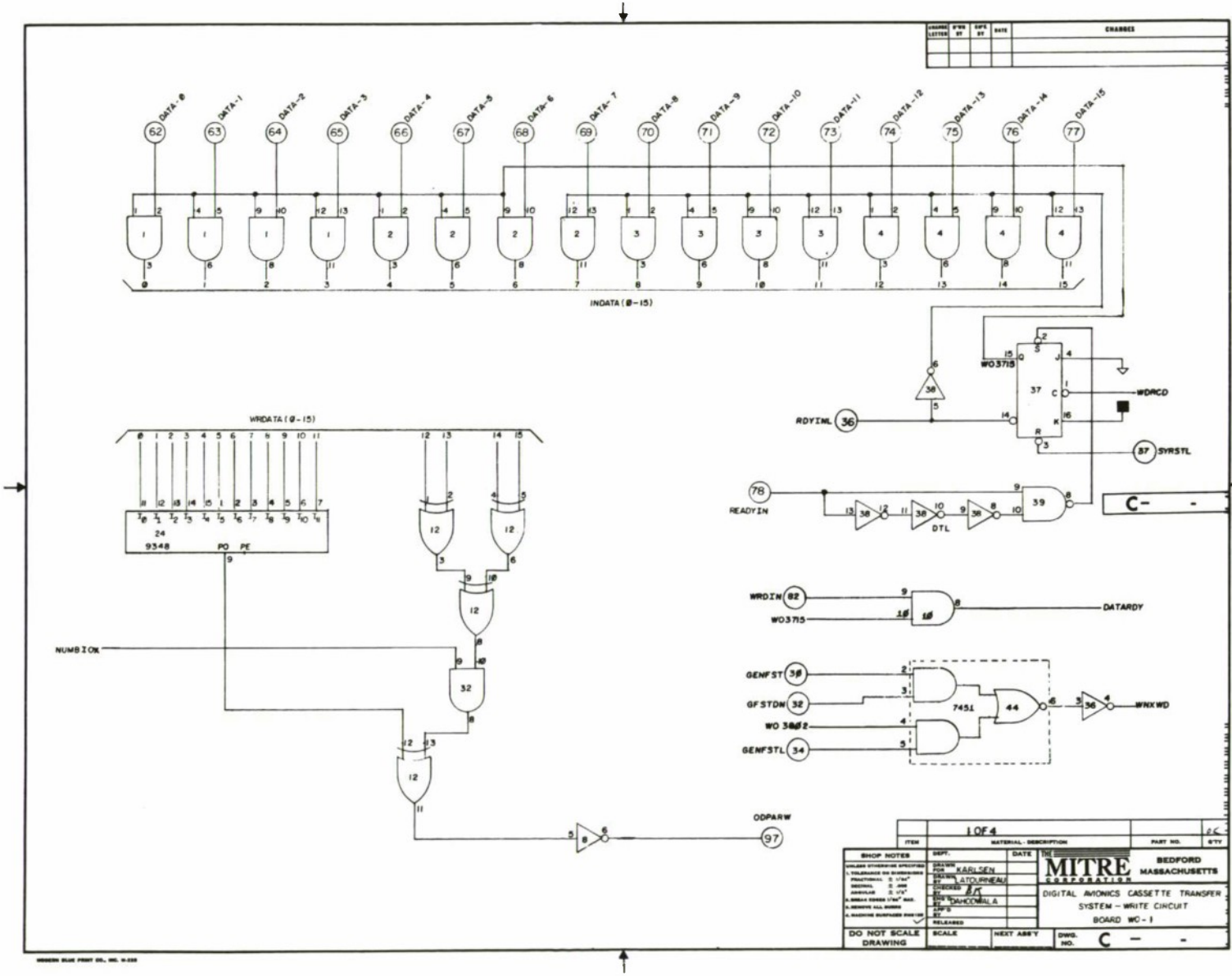


Figure 48 Digital Avionics Cassette Transfer System Write Circuit - Board WO-1

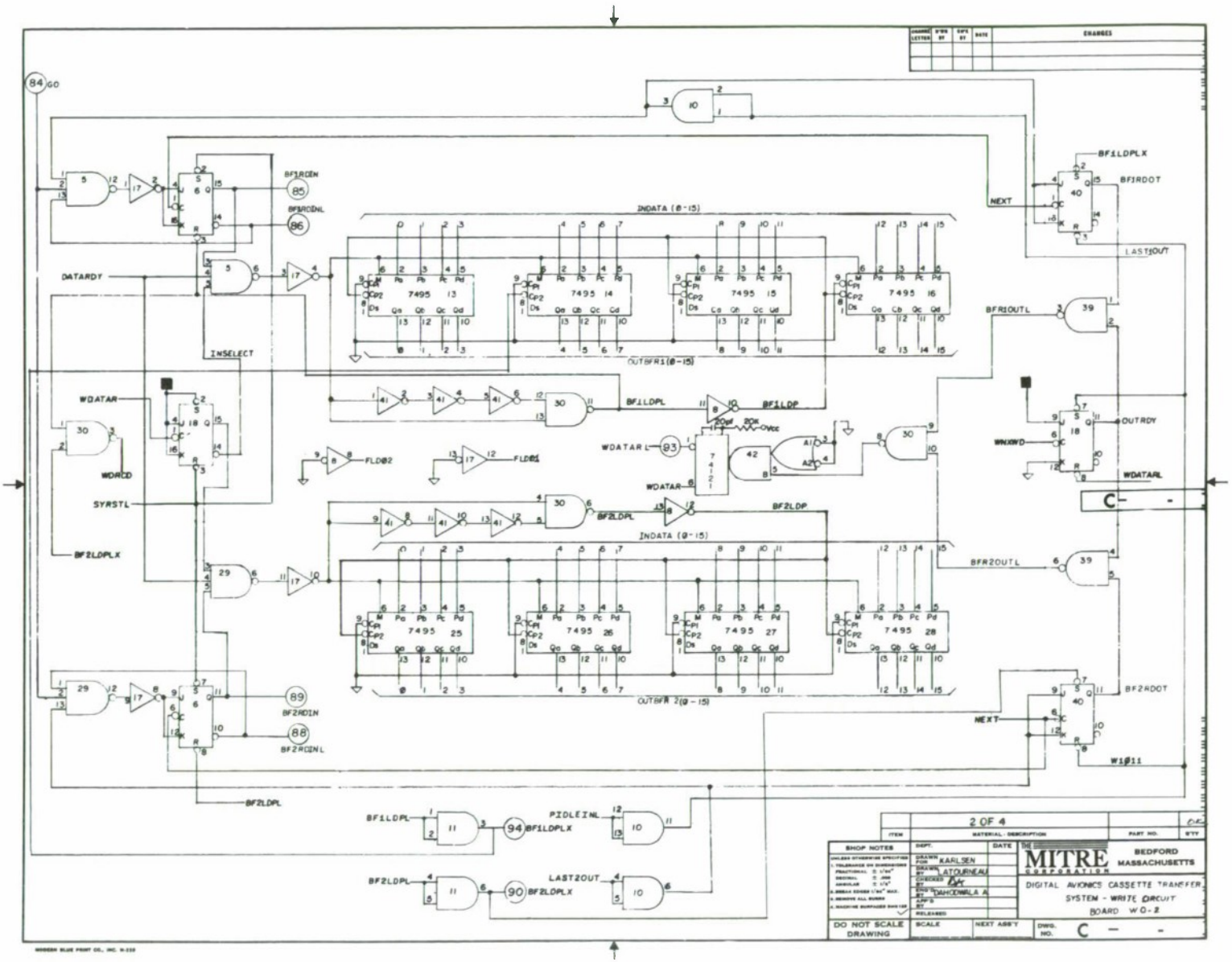


Figure 49 Digital Avionics Cassette Transfer System Write Circuit - Board WO-2

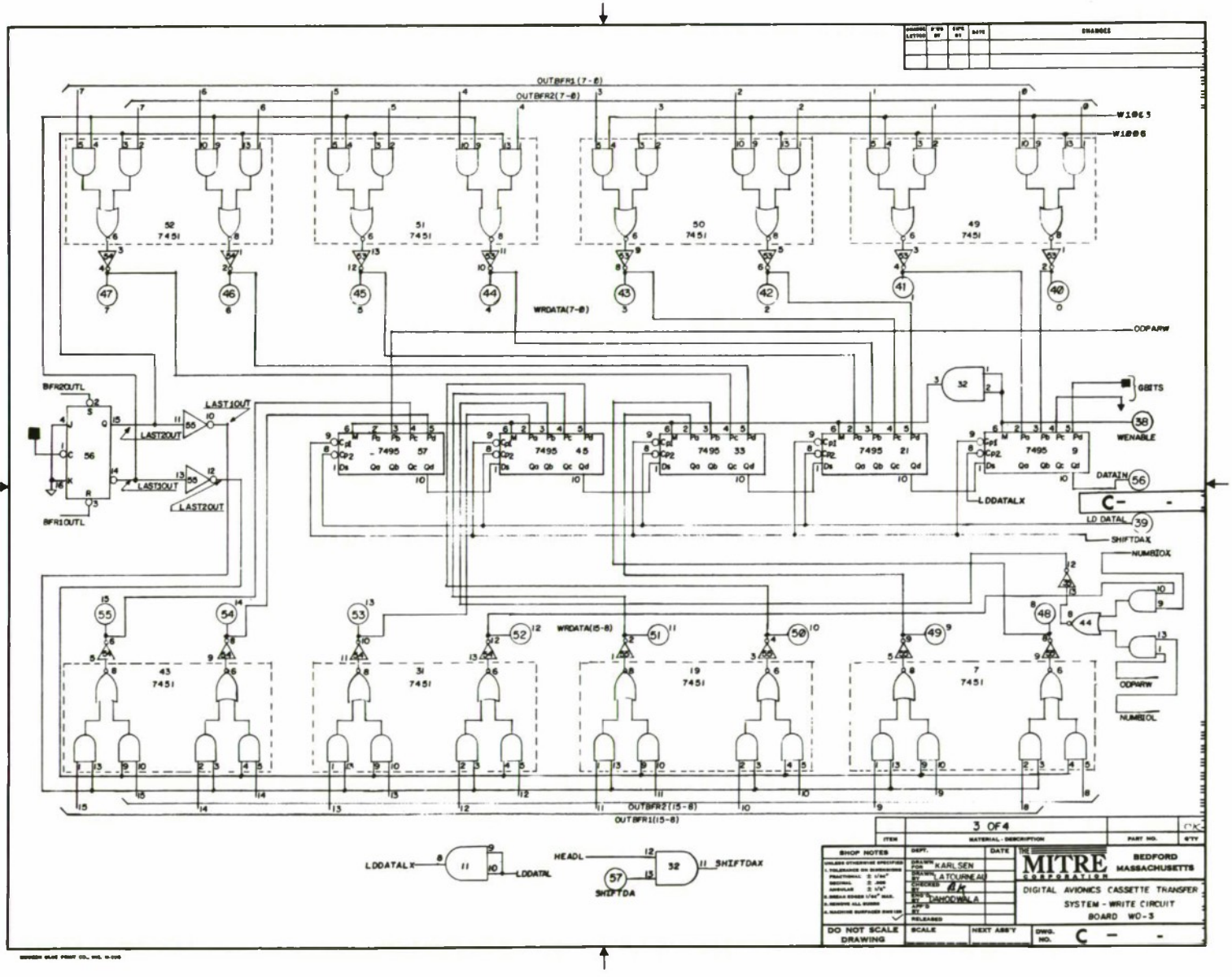


Figure 50 Digital Avionics Cassette Transfer System Write Circuit - Board WO-3

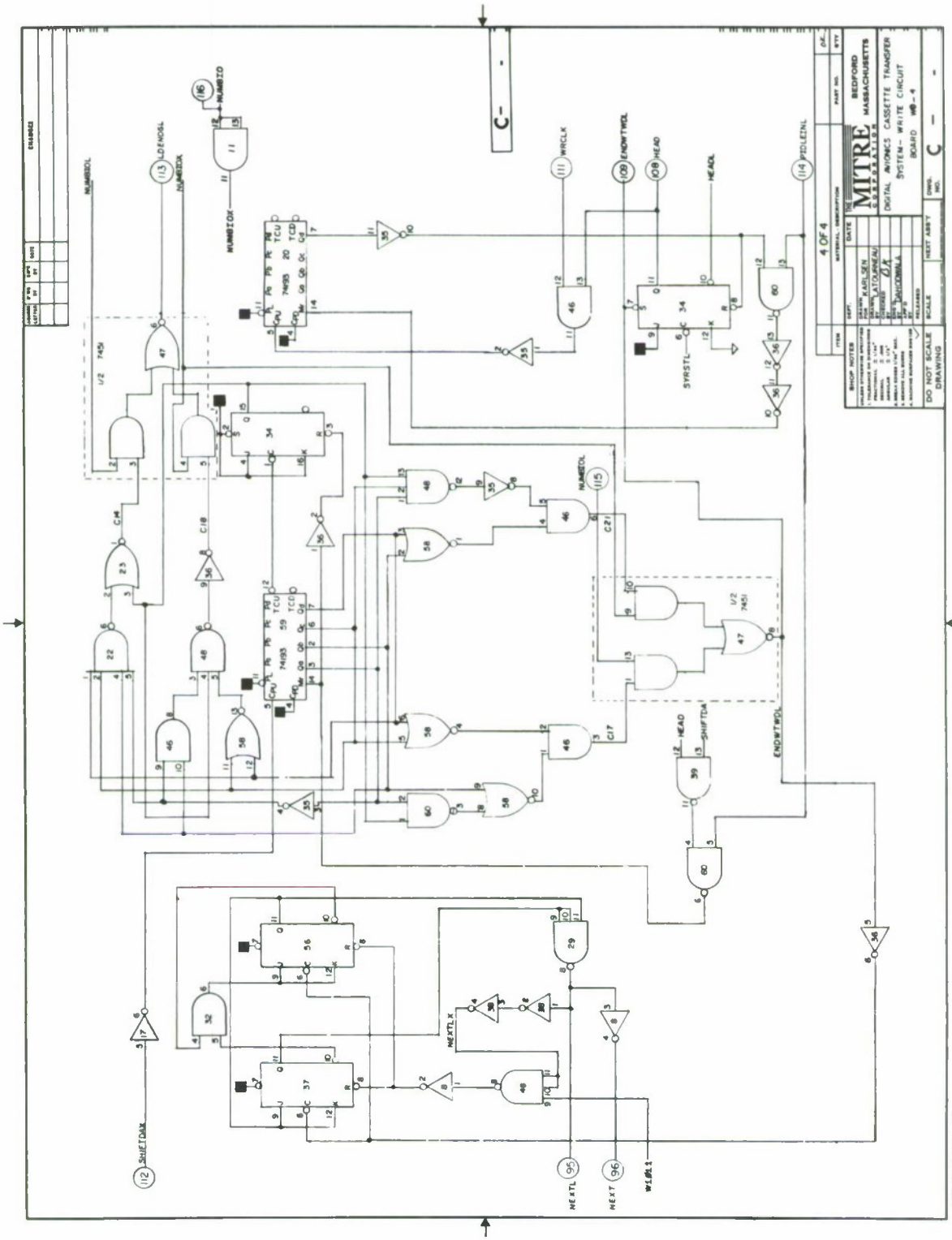


Figure 51 Digital Avionics Cassette Transfer System Write Circuit - Board WO-4

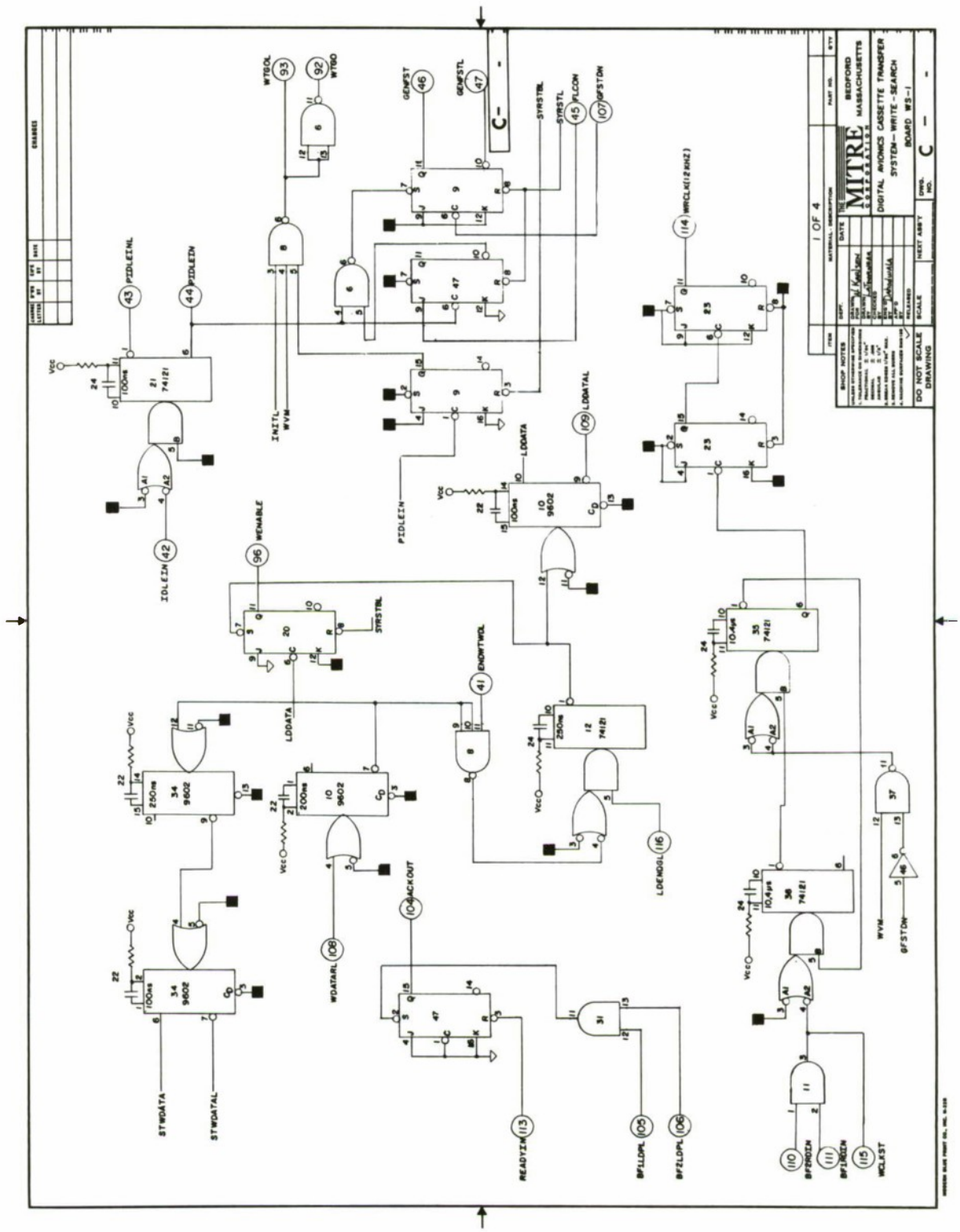


Figure 52 Digital Avionics Cassette Transfer System Write-Search - Board WS-1

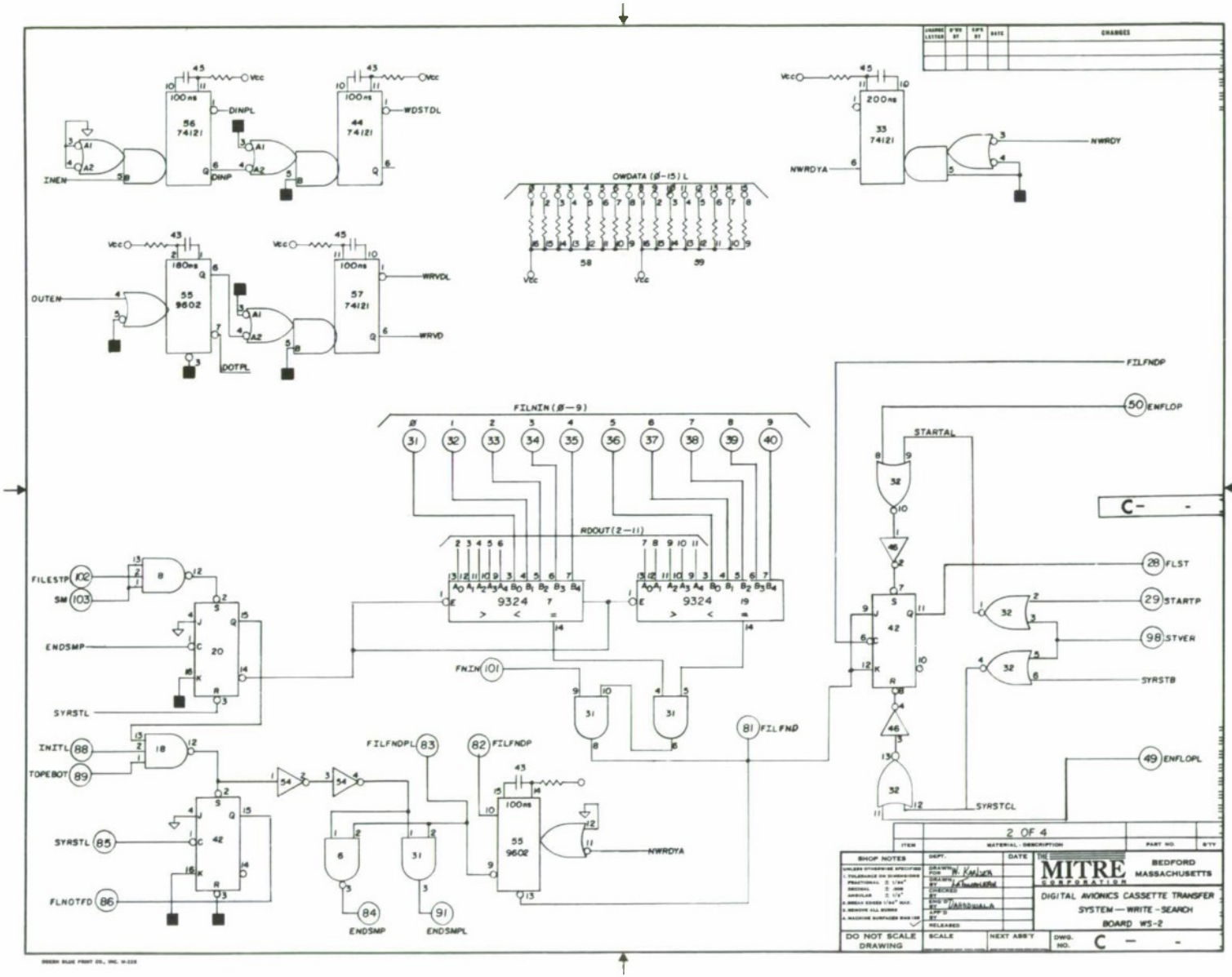


Figure 53 Digital Avionics Cassette Transfer System Write-Search - Board WS-2

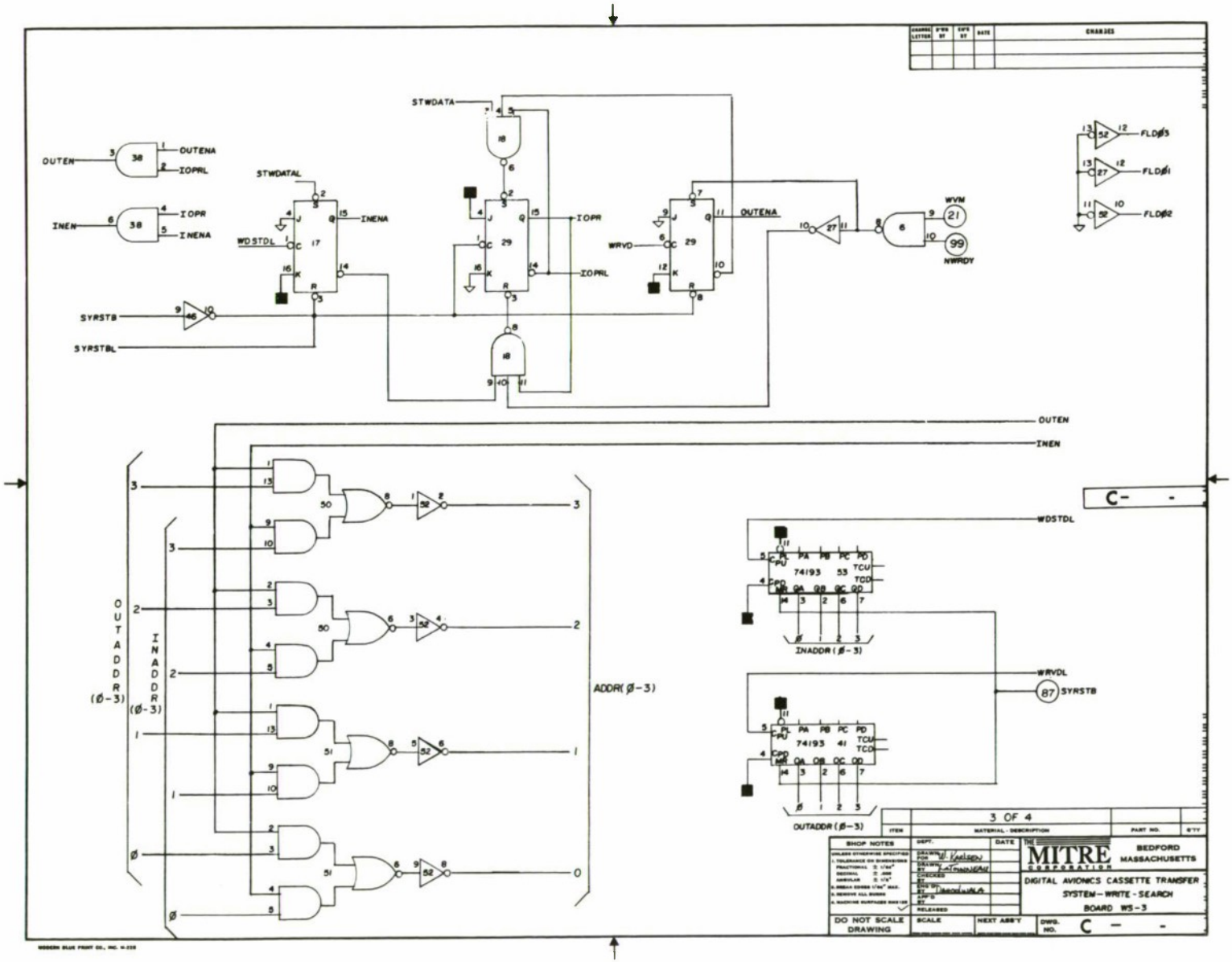


Figure 54 Digital Avionics Cassette Transfer System Write-Search - Board WS-3

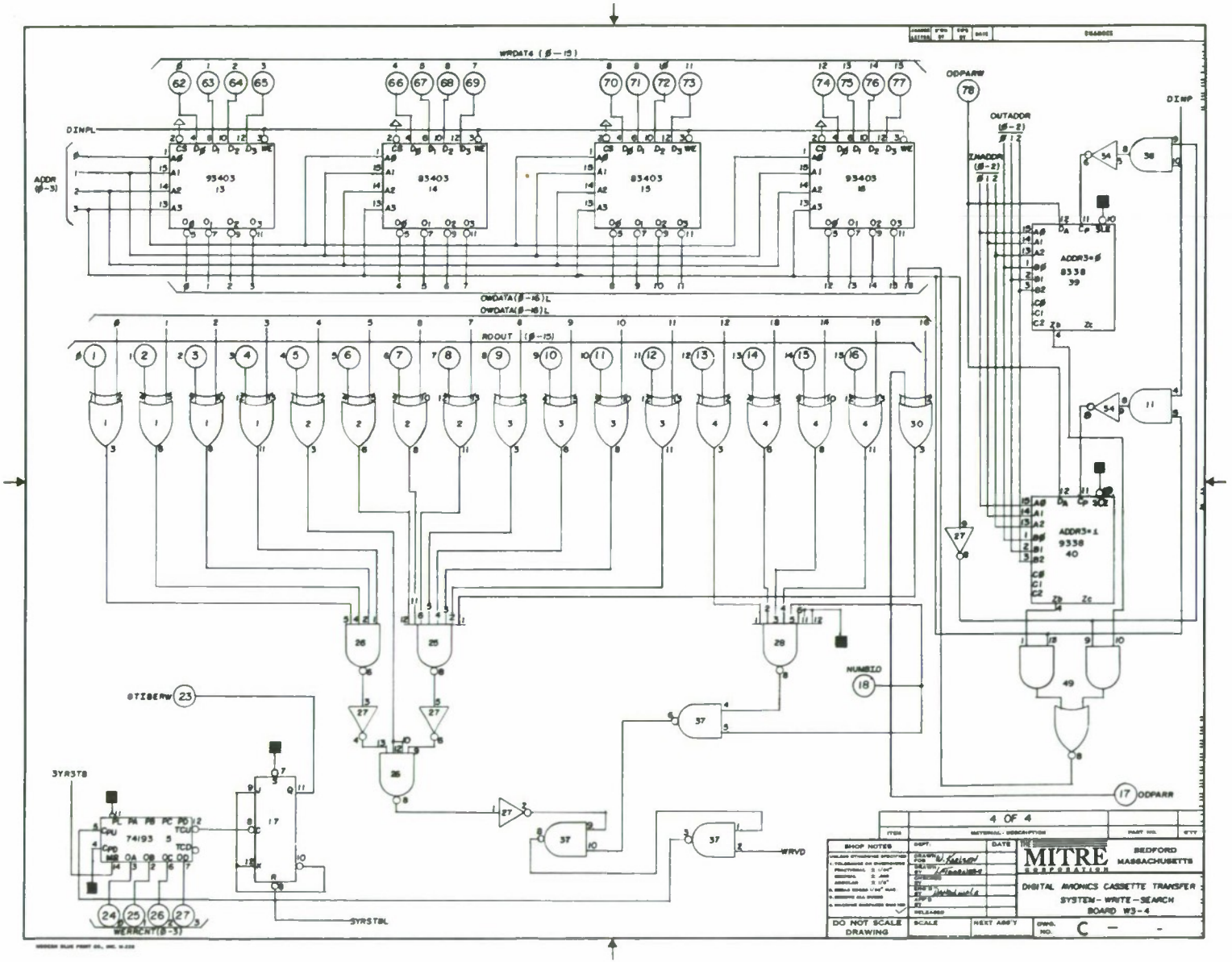


Figure 55 Digital Avionics Cassette Transfer System Write-Search - Board WS-4

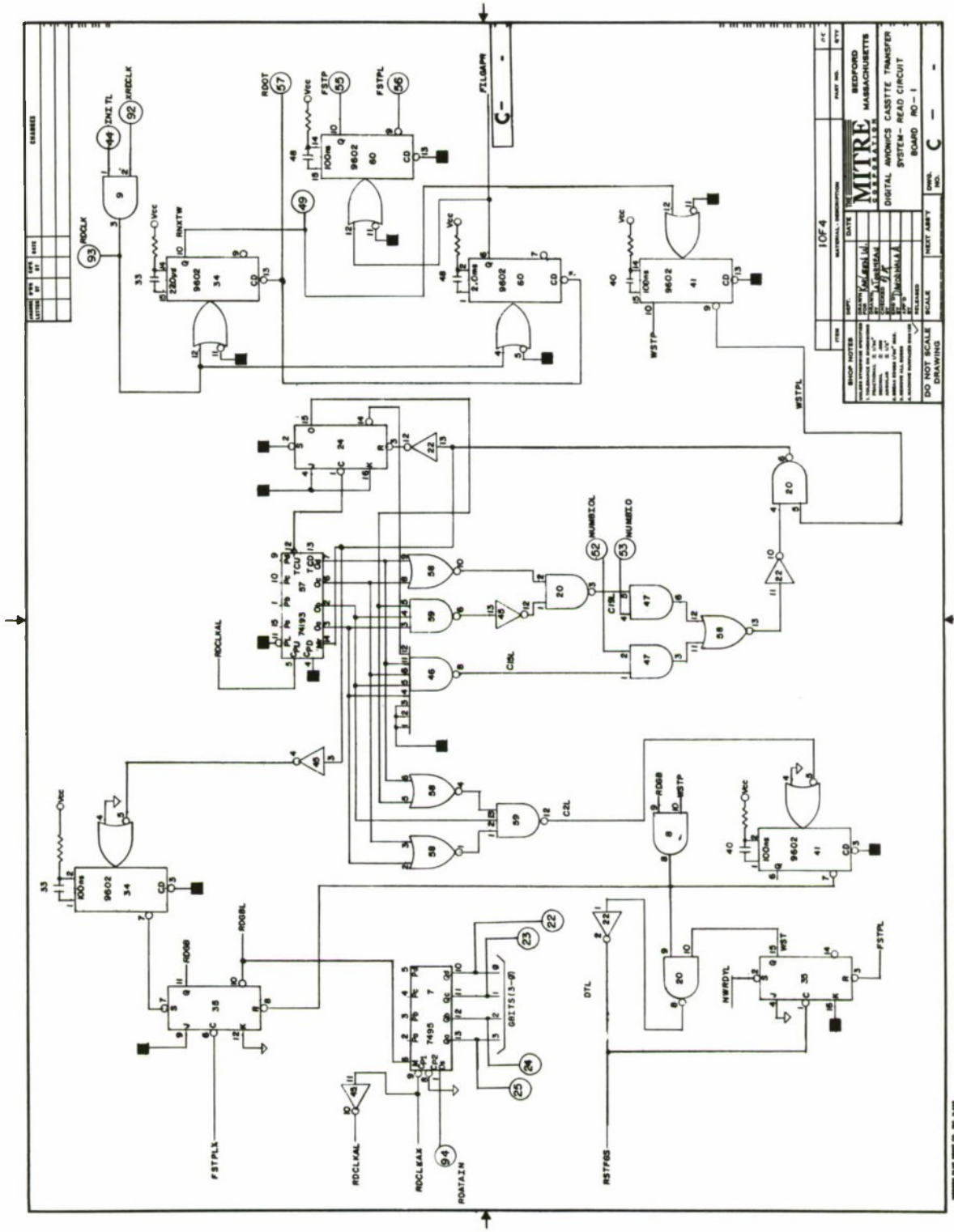


Figure 56 Digital Avionics Cassette Transfer System Read Circuit - Board RO-1

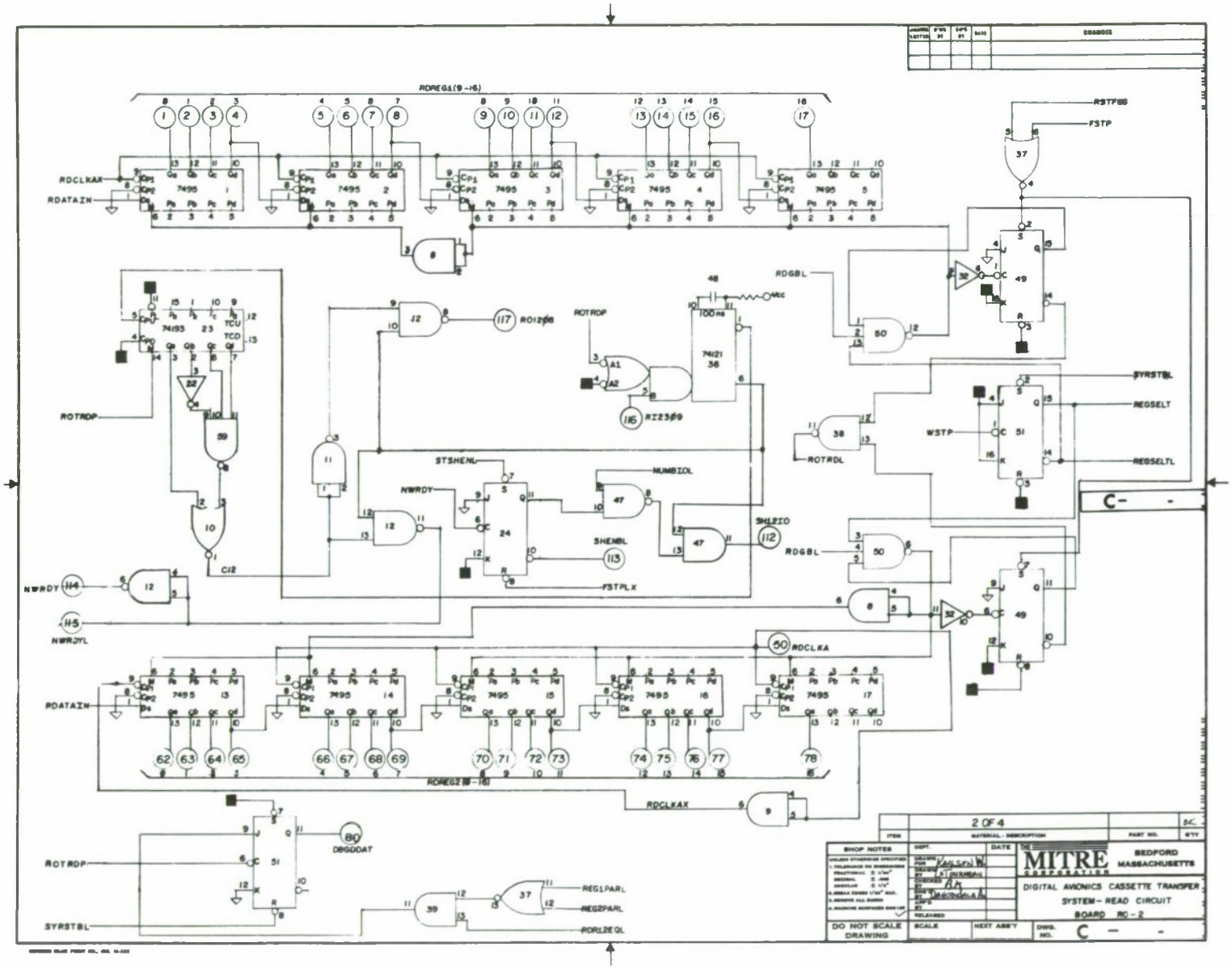


Figure 57 Digital Avionics Cassette Transfer System Read Circuit - Board RO-2

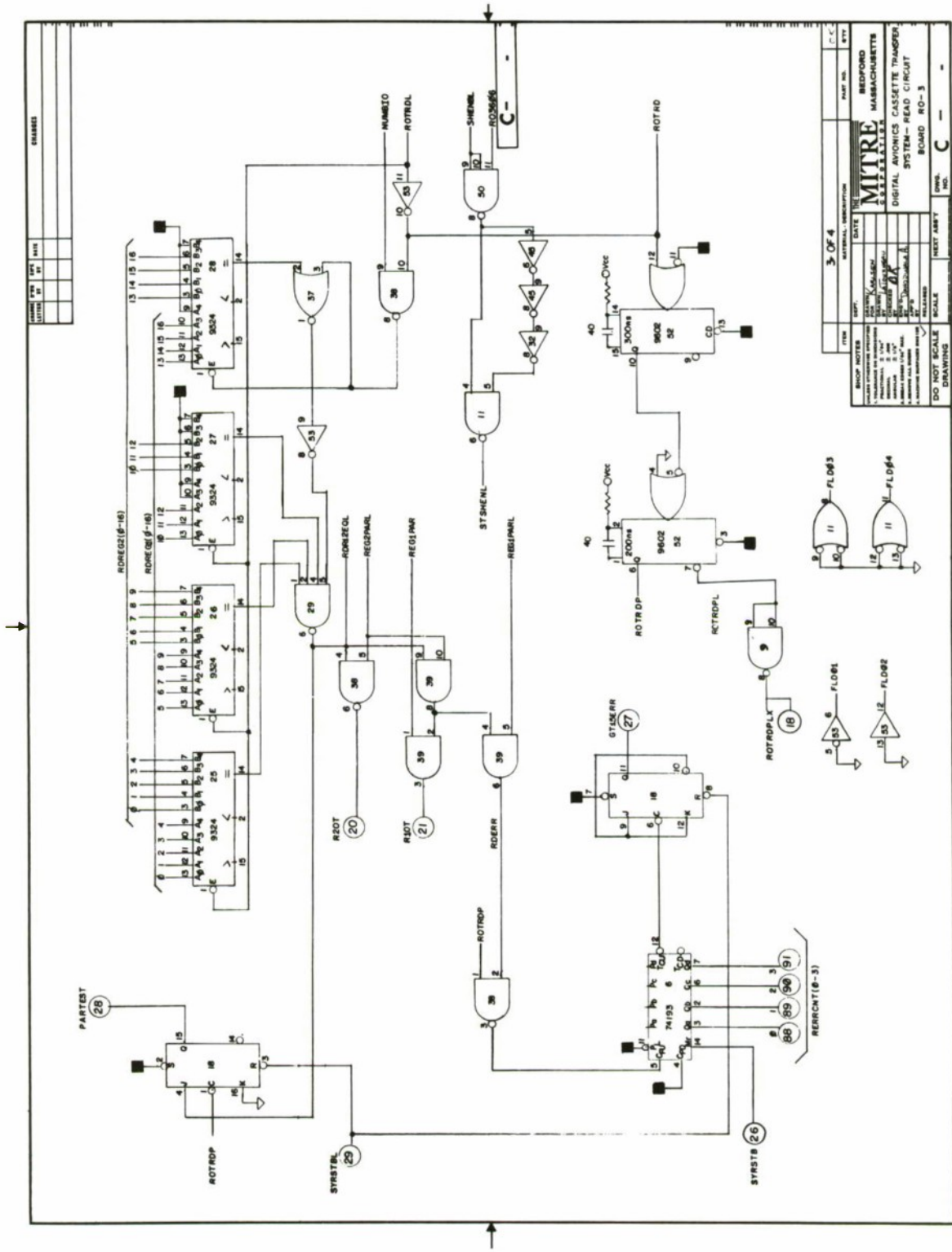


Figure 58 Digital Avionics Cassette Transfer System Read Circuit - Board RO-3

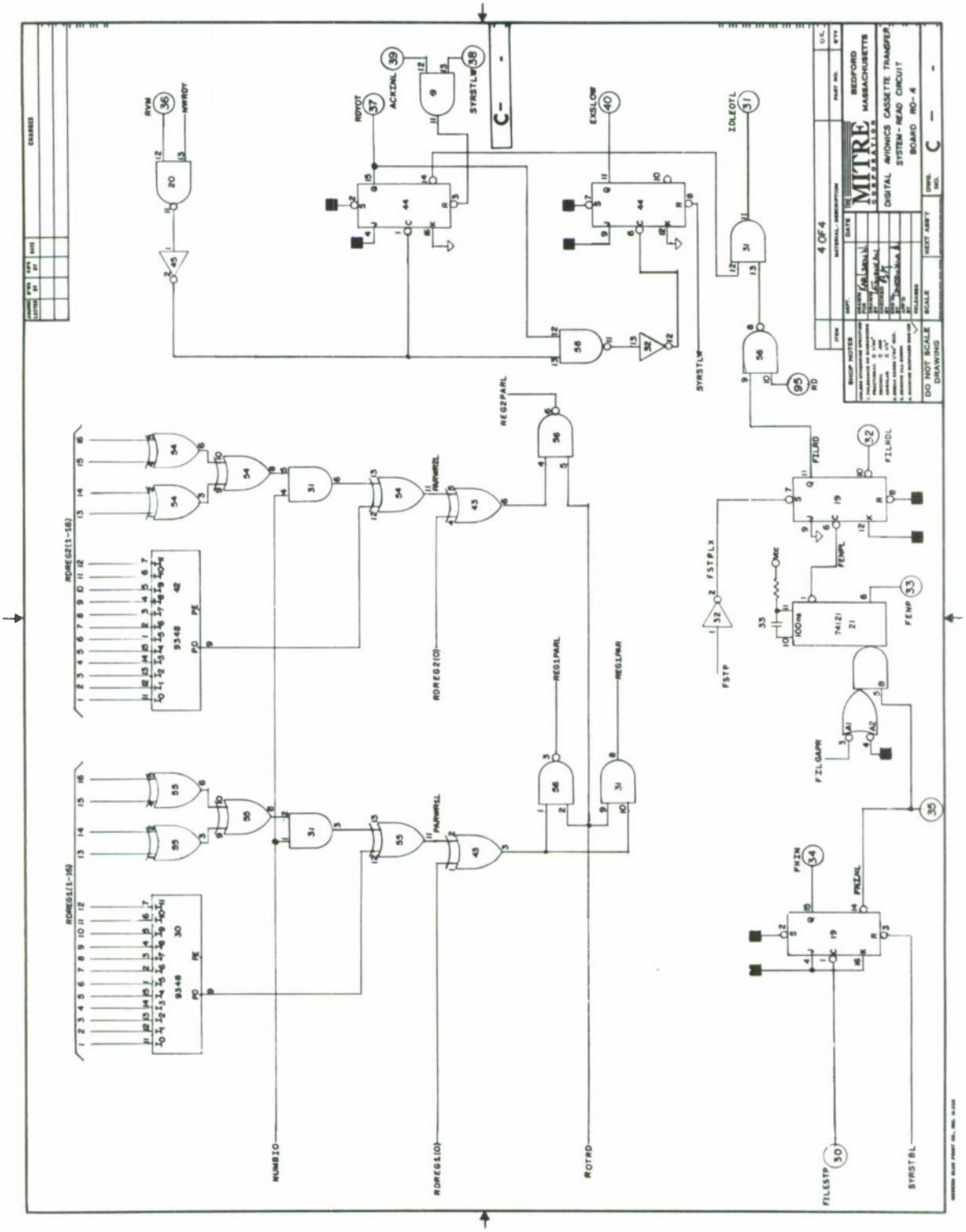


Figure 59 Digital Avionics Cassette Transfer System Read Circuit - Board RO-4

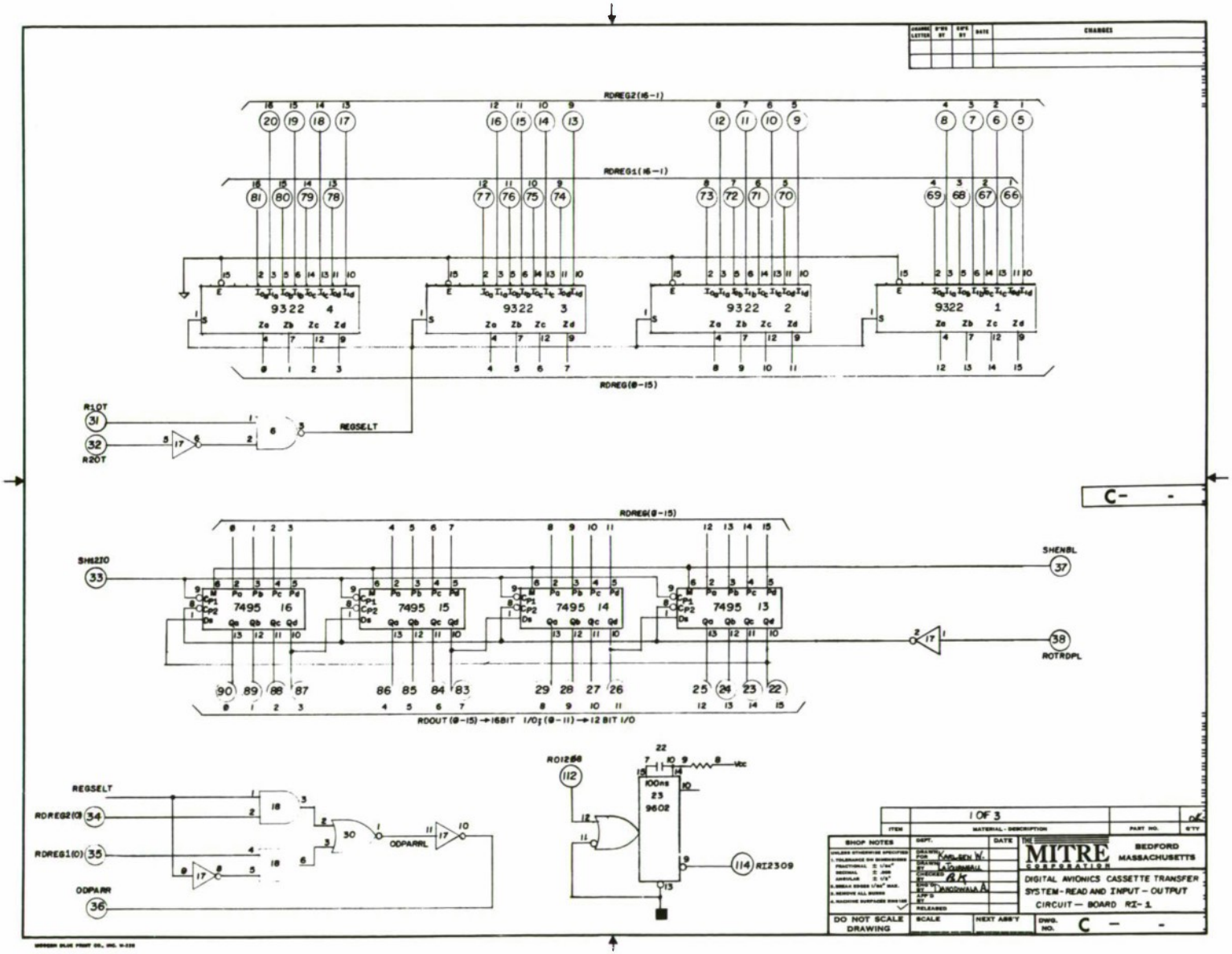


Figure 60 Digital Avionics Cassette Transfer System Read and Input-Output Circuit - Board RI-1

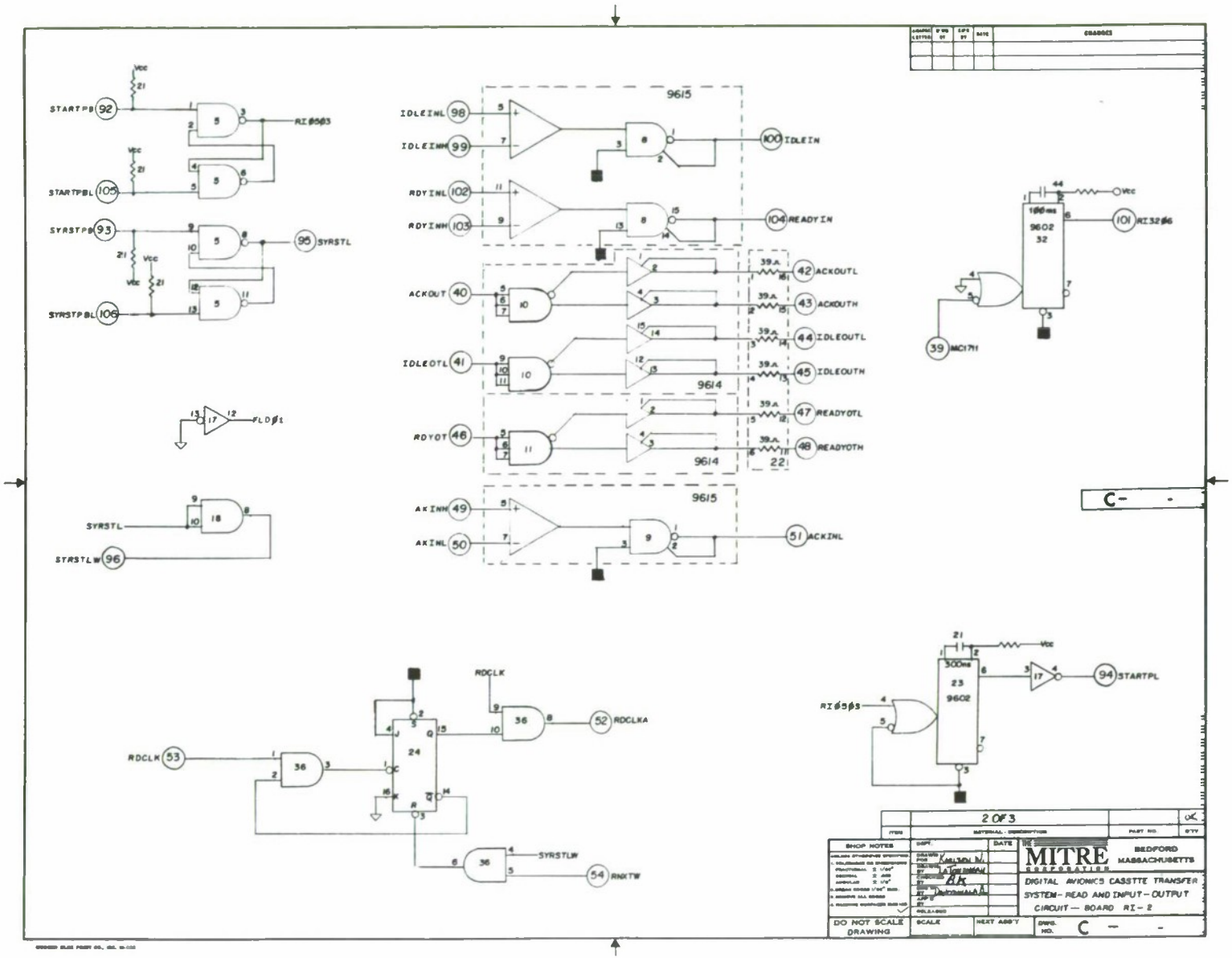


Figure 61 Digital Avionics Cassette Transfer System Read and Input-Output Circuit - Board RI-2

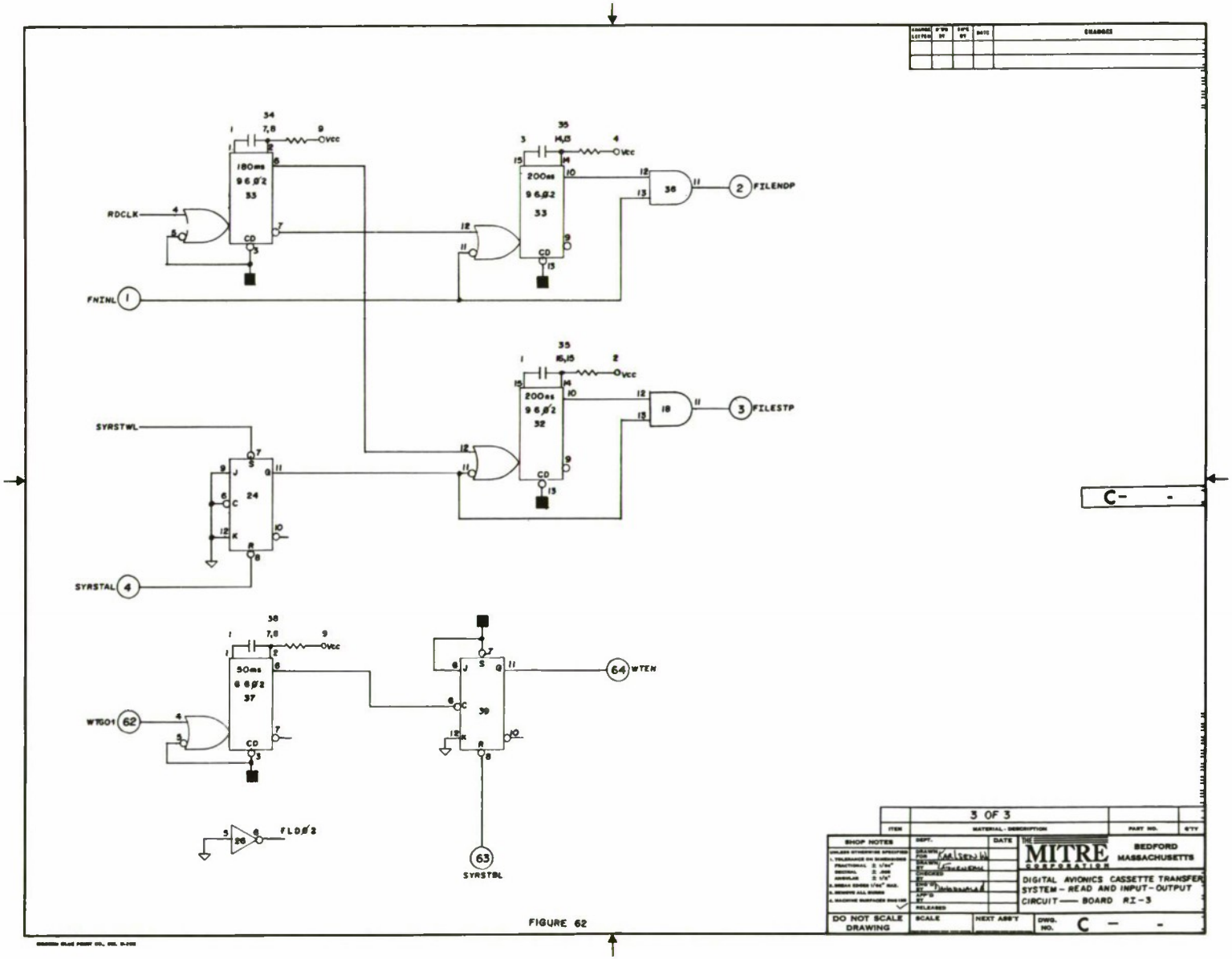


FIGURE 62

Figure 62 Digital Avionics Cassette Transfer System Read and Input-Output Circuit - Board RI-3

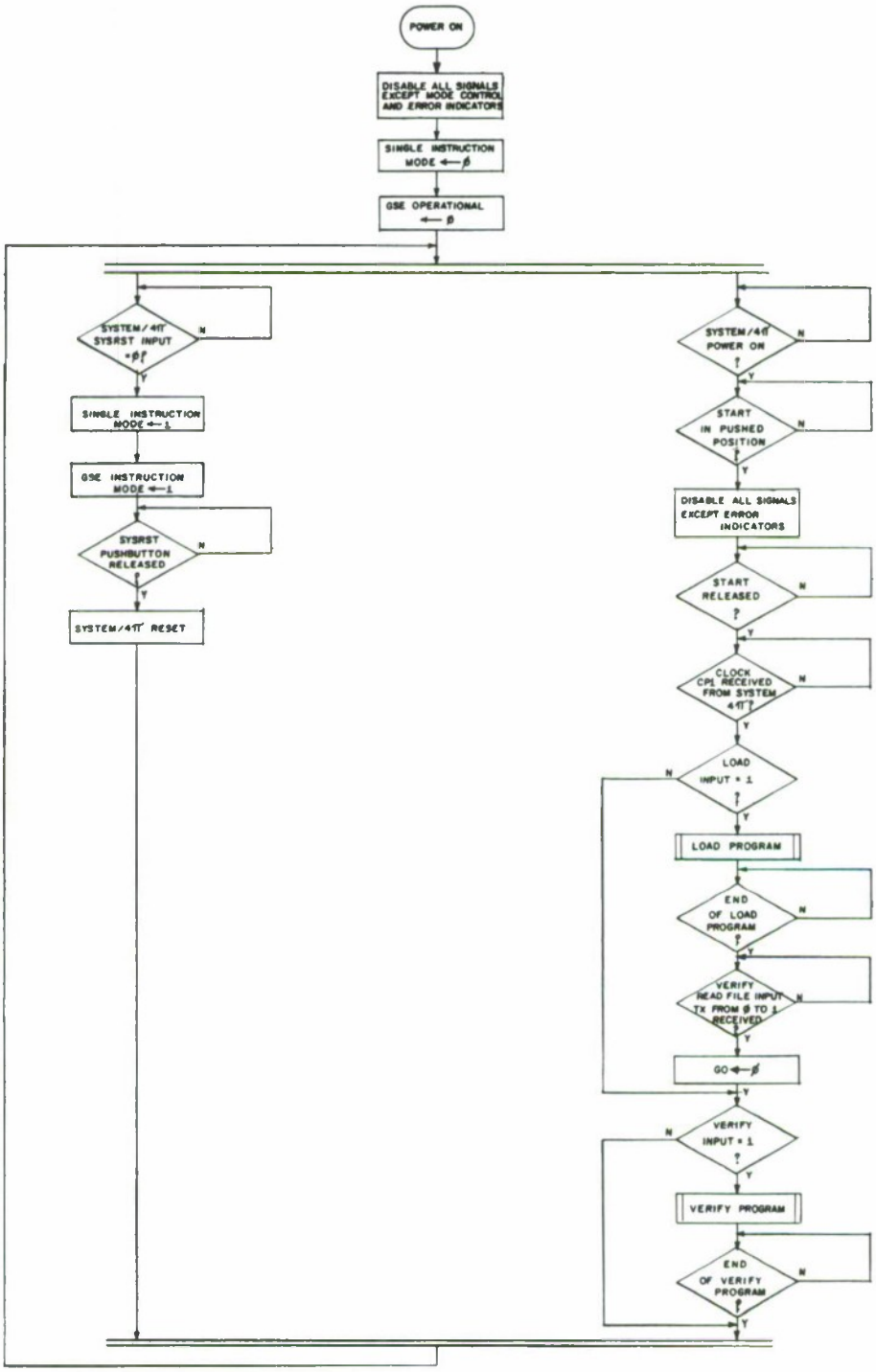


Figure 63 AGE Master Control Program

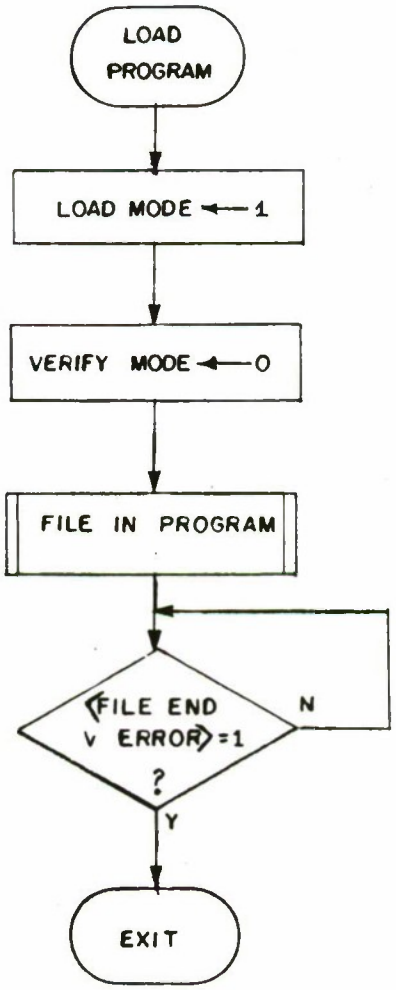


Figure 64 Load Program

File In Program (Figure 65) performs the functions of receiving words from an external device and storing them into System/4Pi CP-2 memory. It calls Input Program which handles the data received. At the end of the Input Program, File In is set and control returns to the calling program if Input Word Received is reset. When Input Word Received is set, it indicates that a word composed of eighteen bits has been assembled by the Input Program. Input Word Received is then reset and two most significant bits of the word are used to determine the type of word. If it is a data word then Storage Protect Bit is loaded from the second most significant bit of the input word and Word Control Program is called. If it is an address then the sixteen least significant bits of the input word are loaded into Current Address Register. If it is neither a data word nor an address word then Error is enabled and control is transferred to the calling program. After the word has been loaded for a data word or the Current Address Register has been updated for an address word, the Output Ready and Input Ready corresponding to the register from which the input word was obtained are respectively reset and set. Out Ready is set, Next Word Pulse is generated and the unit waits until Input Word Received is set again.

Input Program (Figure 66) receives information from an external device through the input connector, converts twelve/sixteen bit words into eighteen bit words and stores it in one of the two input registers. When GO is Ø and Input Idle transition from 1 to Ø has been received, File Name In and GO are set and the unit is ready to receive words. If File Name In is set when Input Ready transitions from Ø to 1 then it indicates that the input word is a File Name. Bit Ø1 of the input word is then stored into I/O Bits and Out Acknowledge is generated as explained later. This bit indicates if the input word size is twelve/sixteen bits. When File Name In is Ø and Input Ready transitions from Ø to 1 then it indicates that the input word is part of the information to be used to store data into System/4Pi CP-2 memory. The input word is converted into a serial bit stream with one bit shifted out every CP1 clock pulses. If Inreg1 Input Ready is set then the serial data is shifted into Inreg1 and Select Input Register is set to 1; otherwise, if Inreg2 Input Ready is set then the serial data is shifted into Inreg2 and Select Input Register is set to 2. At every CP1 clock pulse used to shift data, Shift Bit Count and In Bit Count are incremented by one. When Shift Bit Count equals a count of eighteen, it indicates that an eighteen-bit word has been assembled. Input Ready and Output Ready corresponding to the register into which data was shifted are respectively reset and set. When Out Ready is set, it indi-

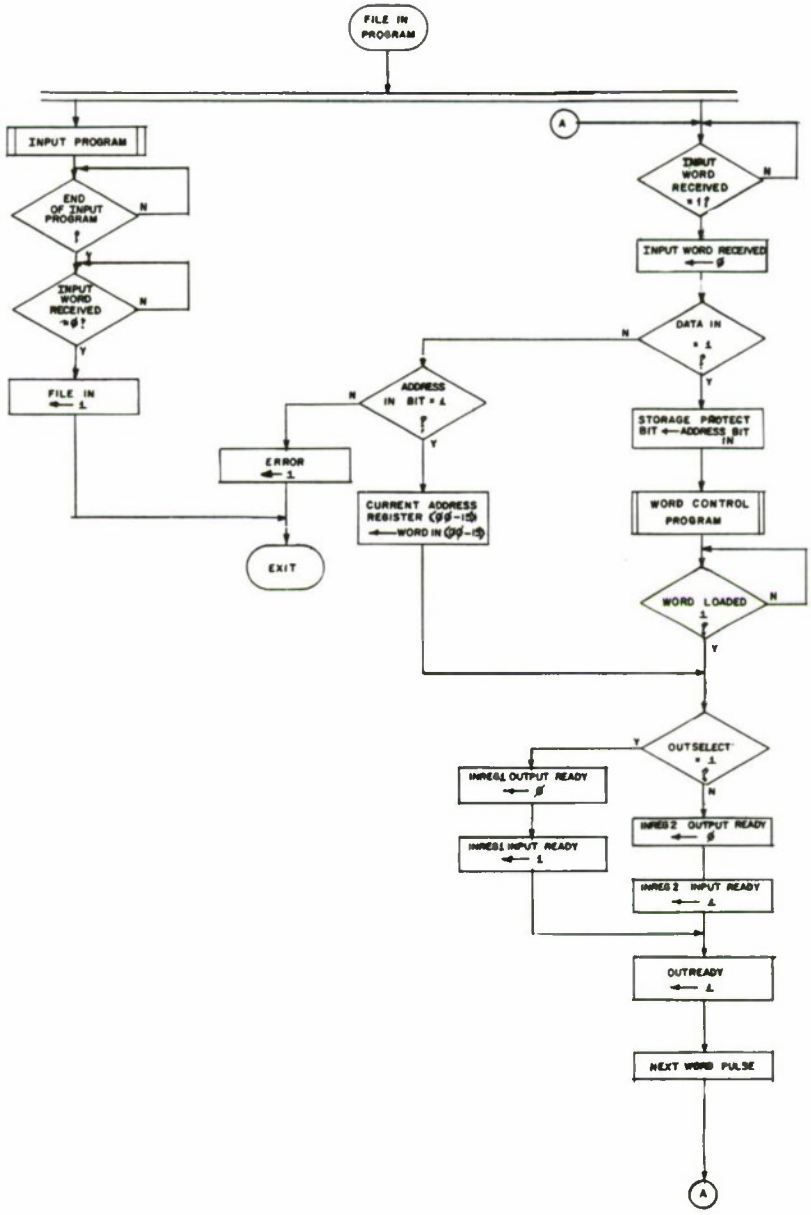


Figure 65 File In Program

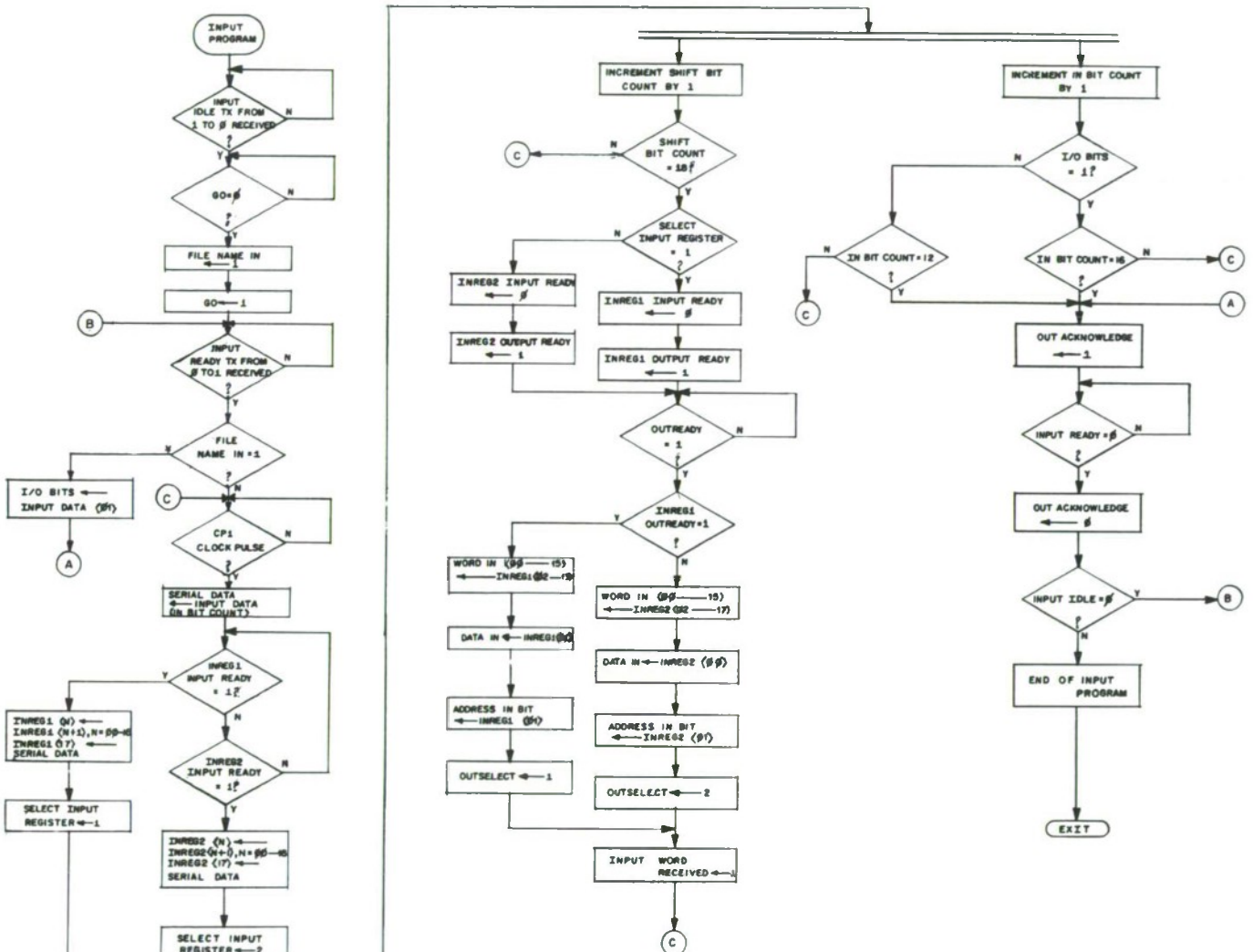


Figure 66 Input Program

cates that File In Program is ready to receive the next eighteen-bit input word. If Inreg1 Output Ready is set then the least significant sixteen bits of Inreg1 become the Word In, Data In equals the most significant bit of Inreg1, Address In Bit equals the second most significant bit of Inreg1 and Out Select is set to 1; otherwise, Inreg2 is used to set up Word In, Data In, Address In Bit and Out Select is set to 2. Next, Input Word Received is set. When Bit Count reaches a count of twelve/sixteen (depending on the input word size) Out Acknowledge is set. When Input Ready goes to Ø, Out Acknowledge is reset. If Input Idle is Ø then the program waits for the next Ø to 1 transition of Input Ready; otherwise, it indicates the end of the Input Program and control is transferred to the calling program.

Word Control Program (Figure 67) explains the functions of the computer interface that loads information into and/or verifies information stored in System/4Pi CP-2 memory. When a word is ready to be loaded into CP-2 memory, GSE to Main Bus is enabled, Control Counter is reset and GSE Out Bus has the content of the Current Address Register. Every CP4 clock pulse, the Control Counter is incremented, Compare Program is called and different control lines are enabled or disabled depending on the mode of operation and the value of the Control Counter. When the Control Counter equals eight, SAR to GSE In is set, Current Address Register is incremented by one, and if Load Mode equals 1, then Word Loaded is set; otherwise, Word Verified is set. GSE to Main Bus is disabled and control is transferred to the calling program.

Compare Program (Figure 68) verifies the value stored in the Storage Address Register and the Storage Data Register. If Control Counter equals three and CP1 clock pulse is received, then GSE In Bus (having the value of the SAR on it) is compared with the Current Address Register. SAR Error is set if the two quantities are unequal. Control is then transferred to the calling program. When Control Counter equals eight and CP1 clock pulse is received, the GSE In Bus (has SDR on it) is compared with the Word In and the Storage Protect Bit (from System/4Pi CP-2) is compared with Out SPB. If the two quantities are unequal then SDR Error is set. Control is then transferred to the calling program.

Verify Program (Figure 69) sets Verify Mode, resets Load Mode and calls the File In Program. At the end of the file or if an error exists in the control bits, program control is transferred to the calling program.

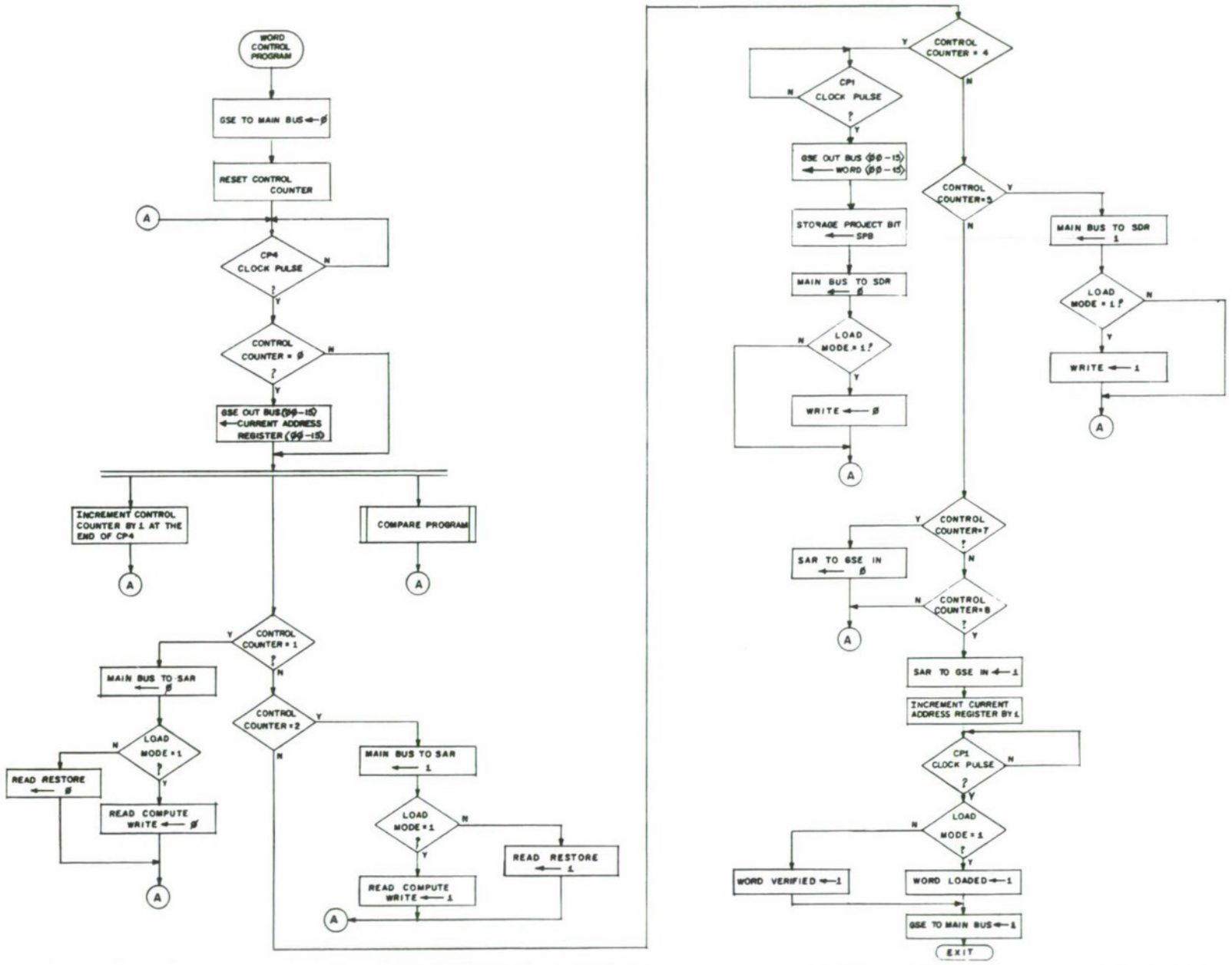


Figure 67 Word Control Program

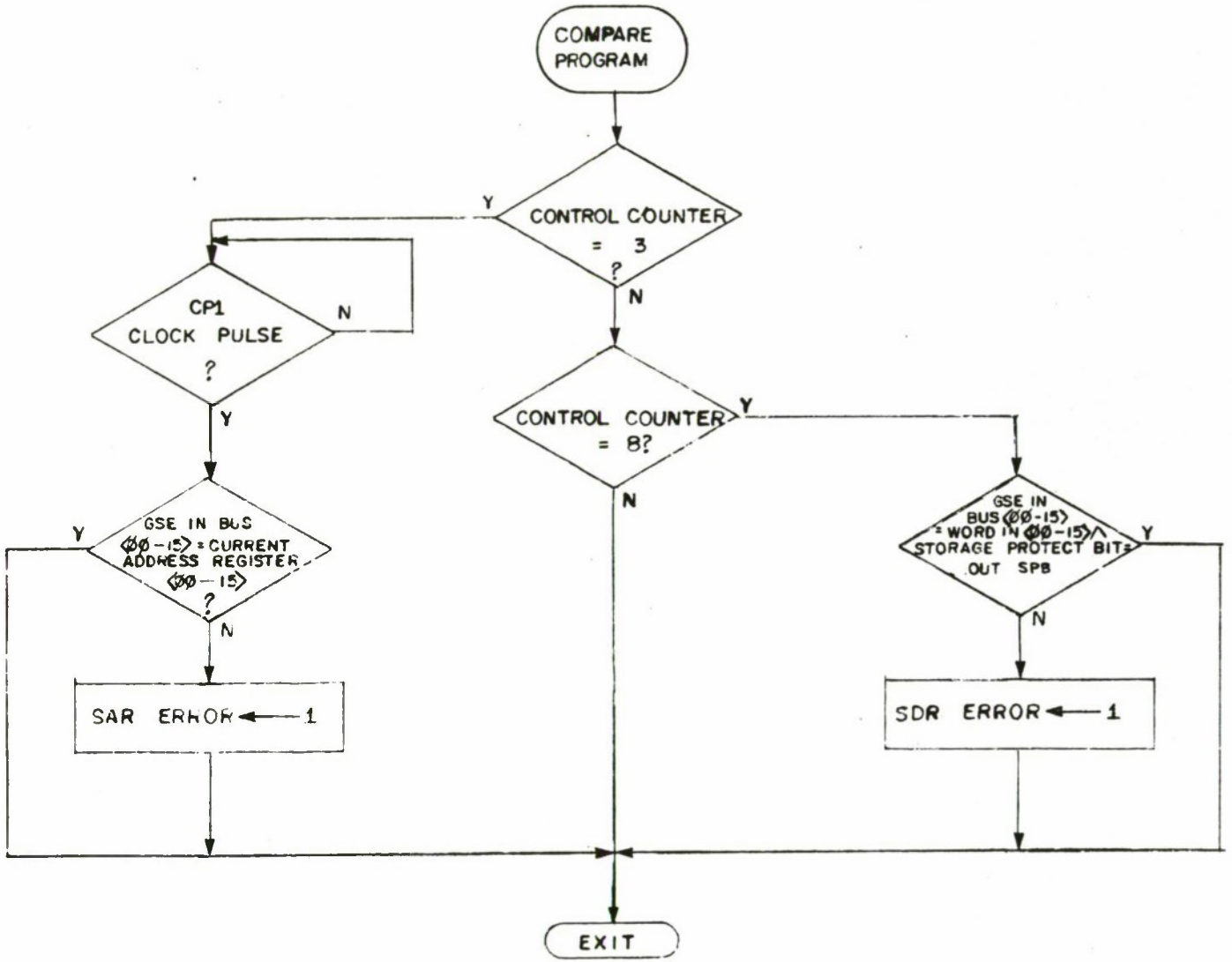


Figure 68 Compare Program

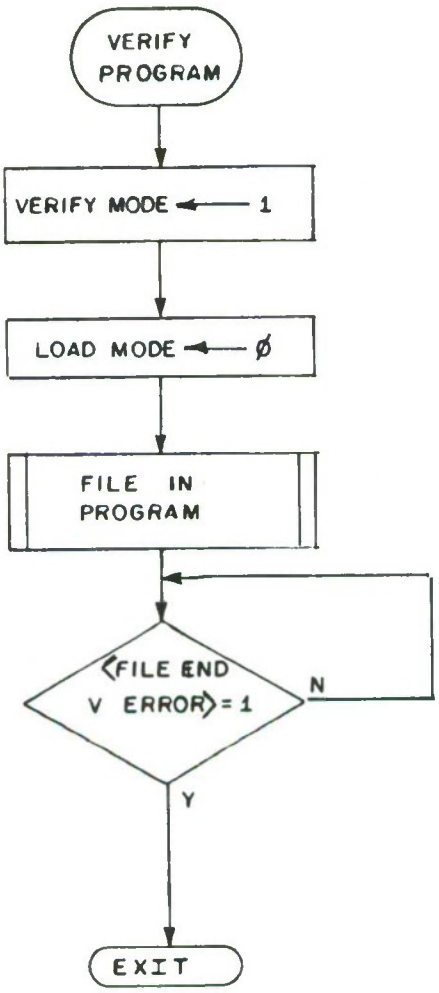


Figure 69 Verify Program

The logic circuit for the AGE Interface is given in Figures 70 to 76.

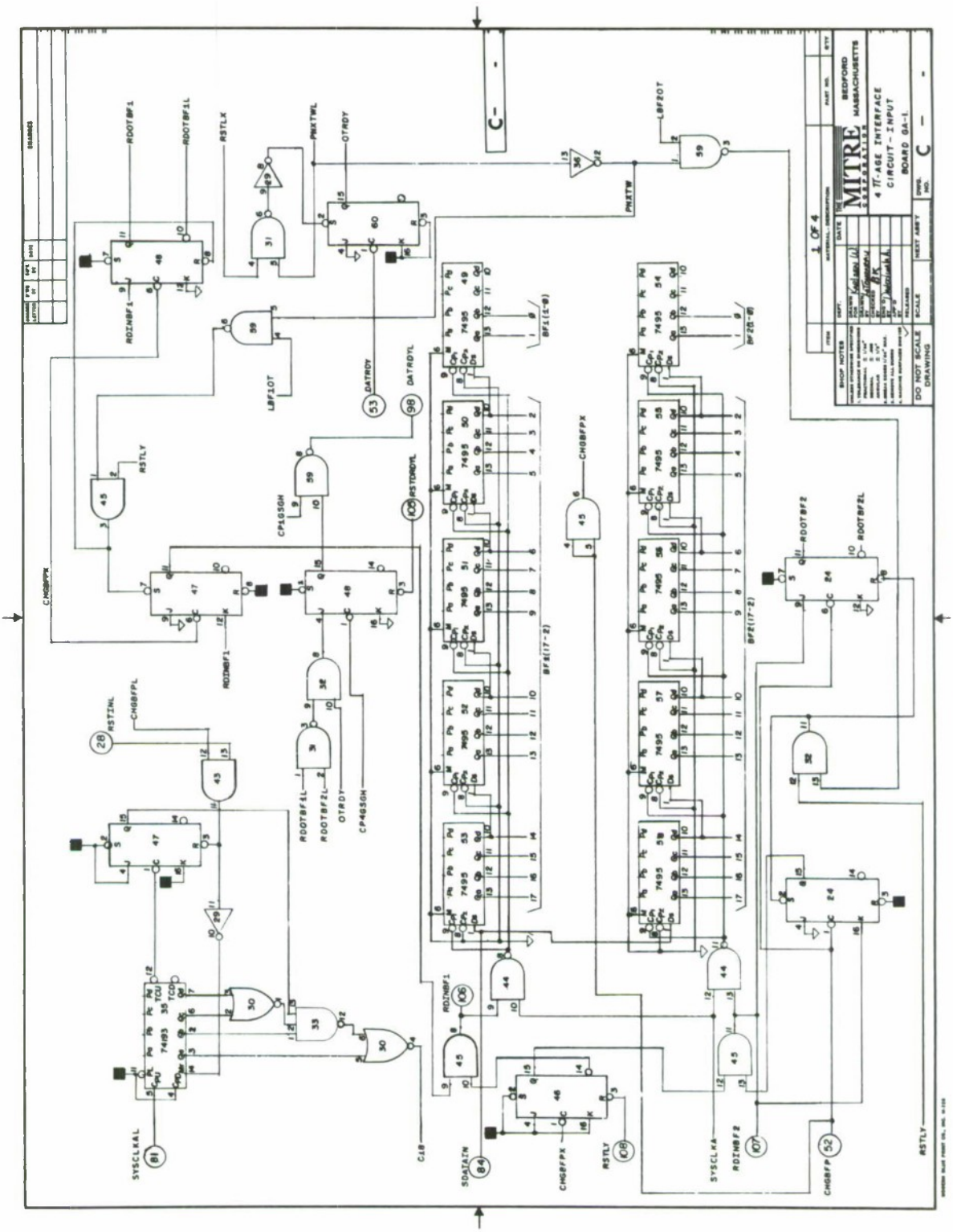


Figure 70 4π-AGE Interface Circuit-Input - Board GA-1

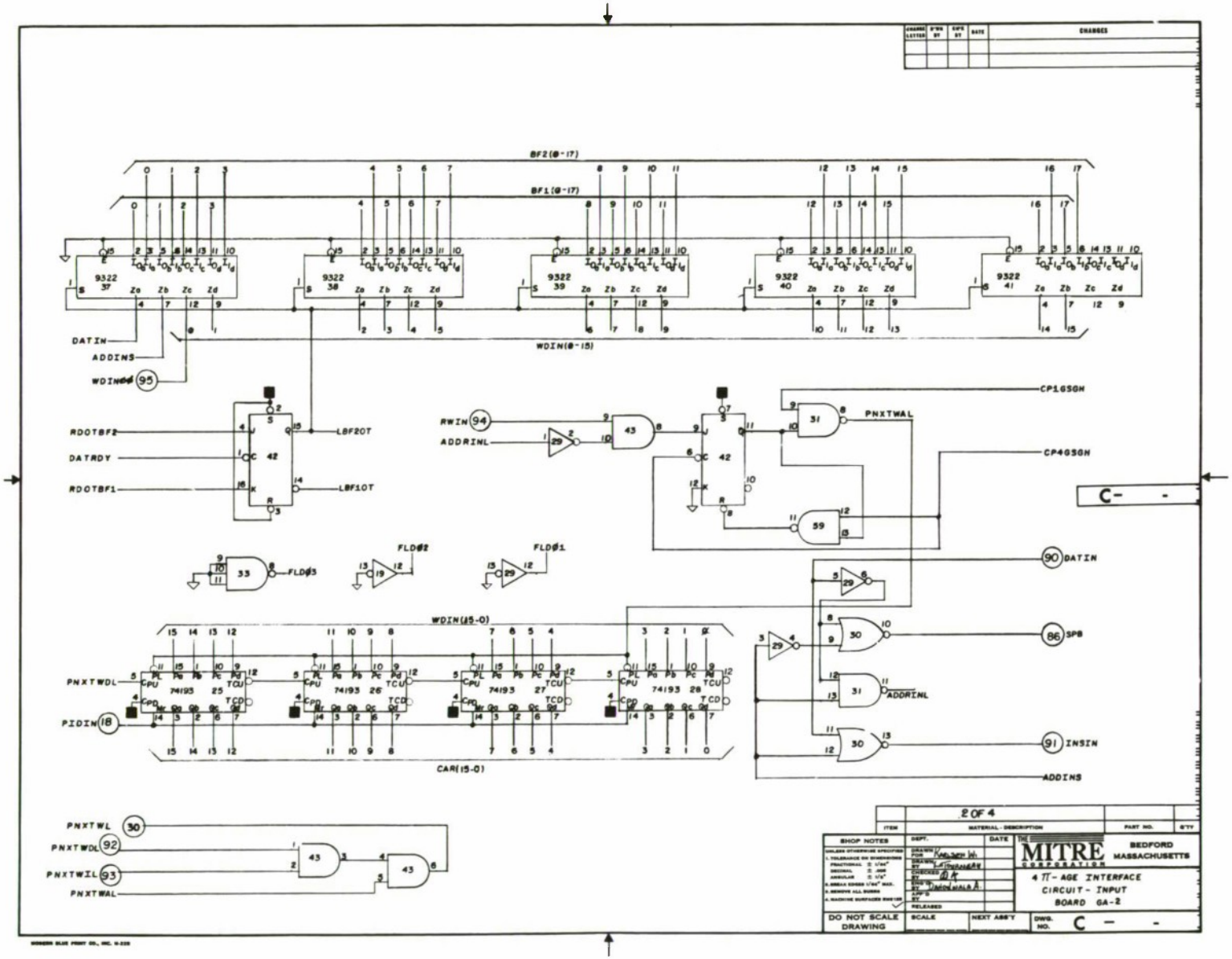


Figure 71 4π-AGE Interface Circuit-Input - Board GA-2

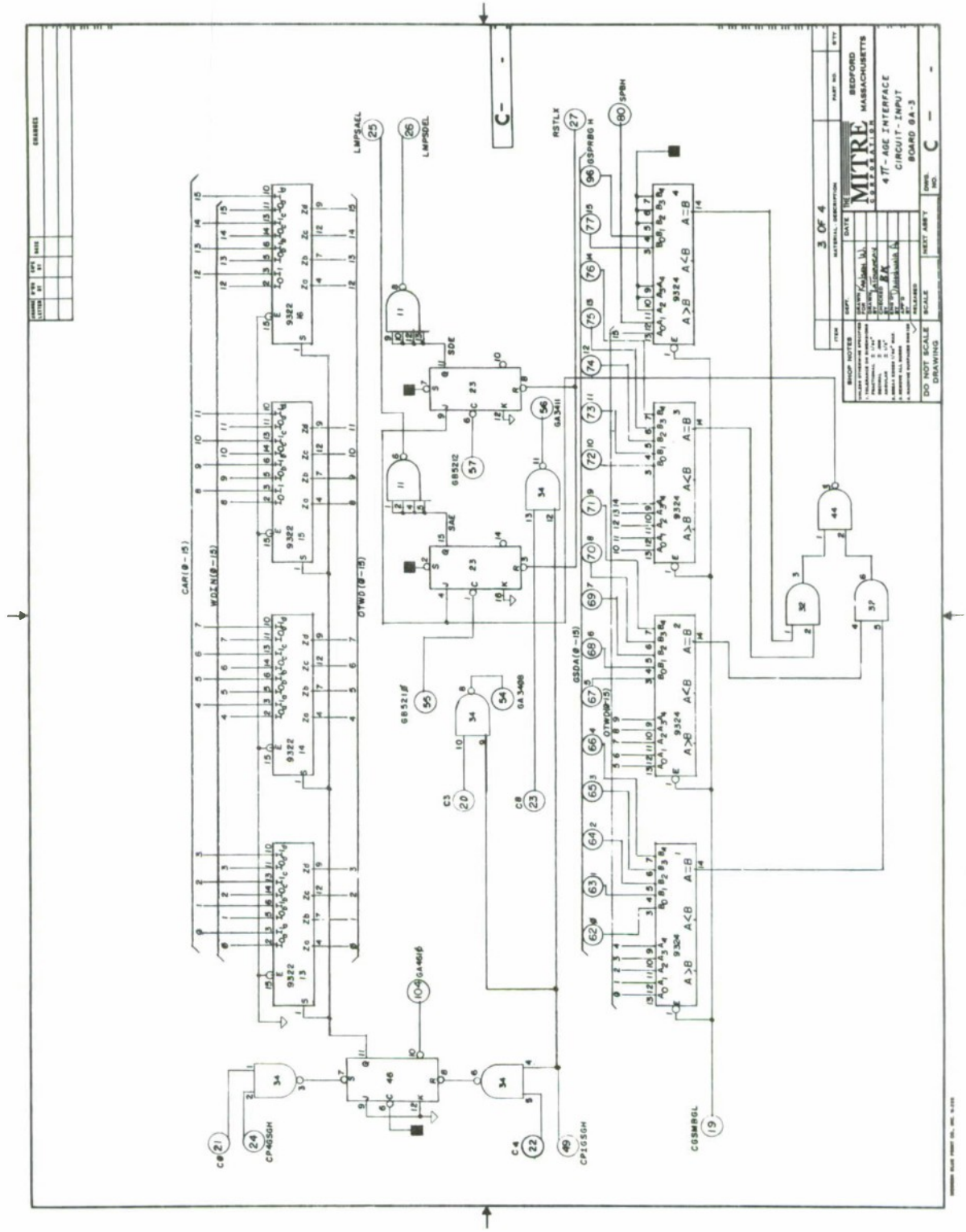


Figure 72 4π-AGE Interface Circuit-Input - Board GA-3

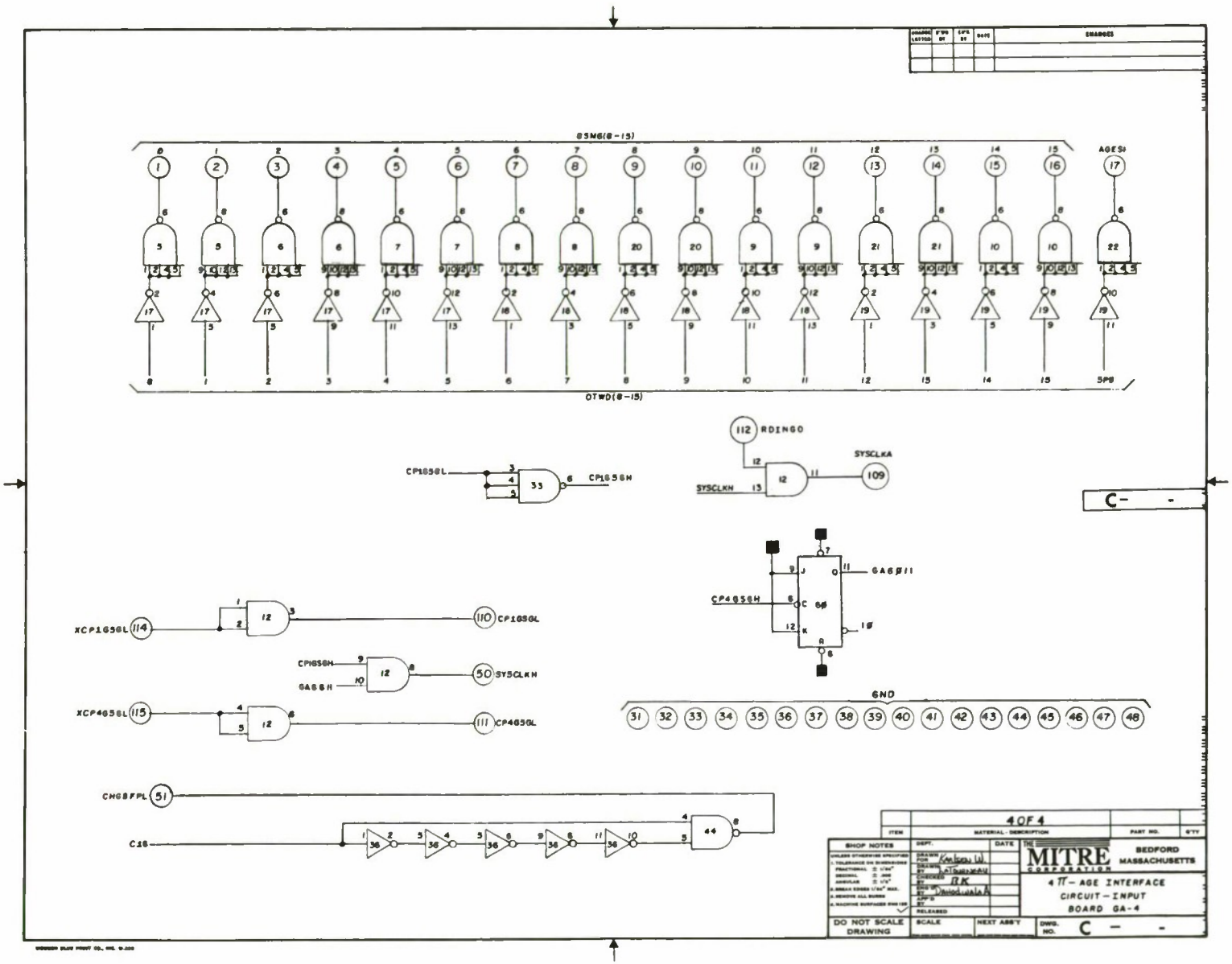


Figure 73 4π-AGE Interface Circuit-Input - Board GA-4

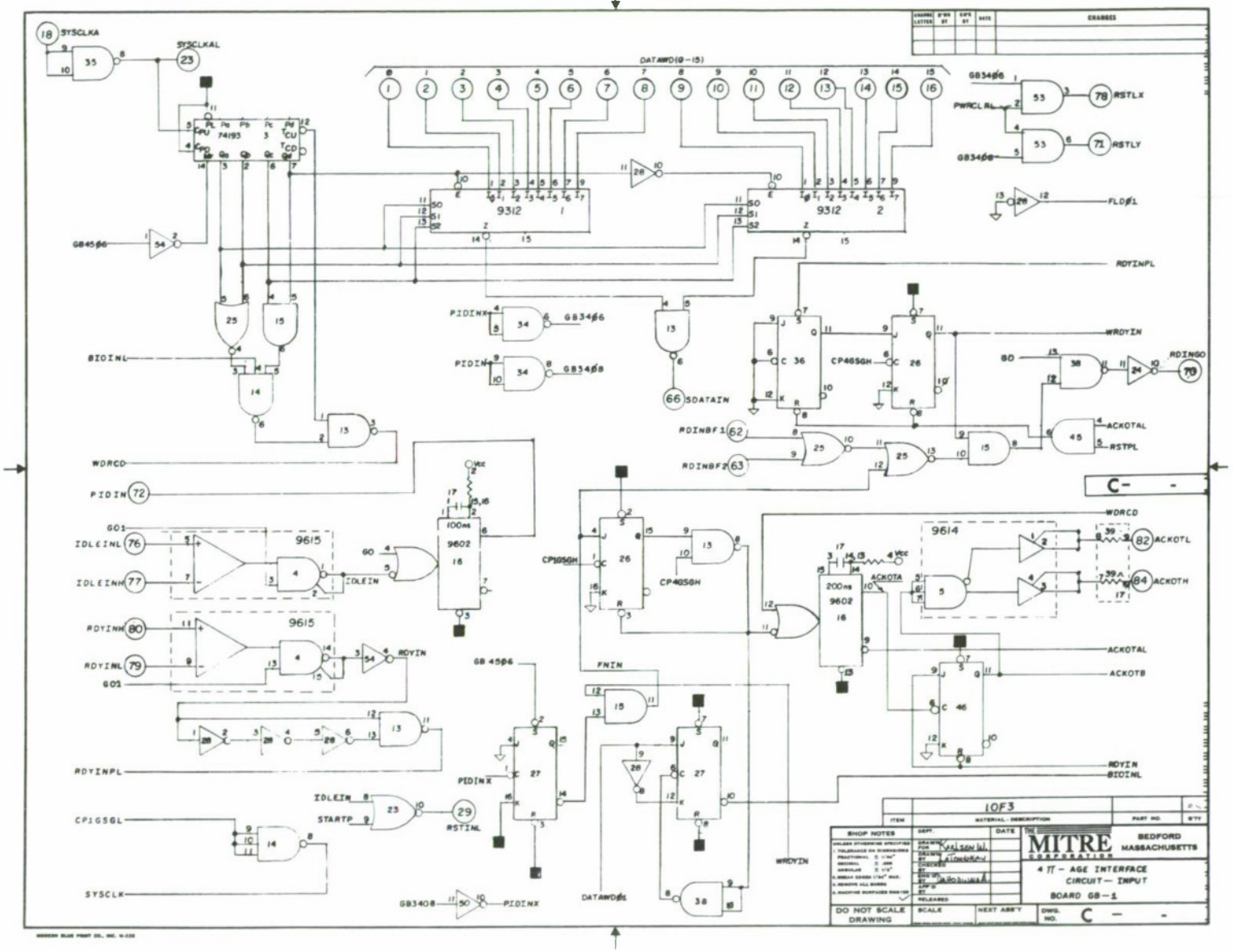


Figure 74 4π-AGE Interface Circuit-Input - Board GB-1

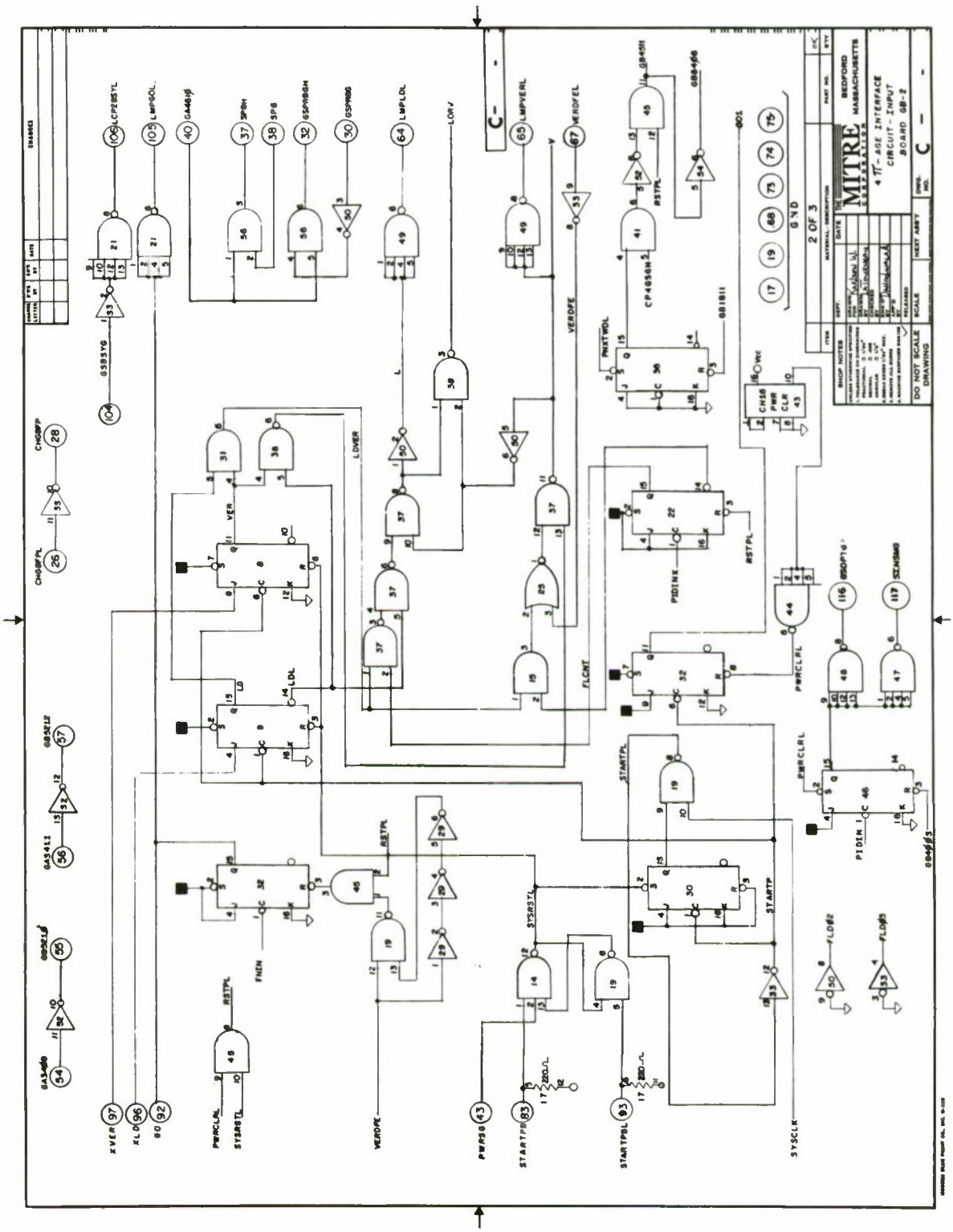


Figure 75 4π-AGE Interface Circuit-Input - Board GB-2

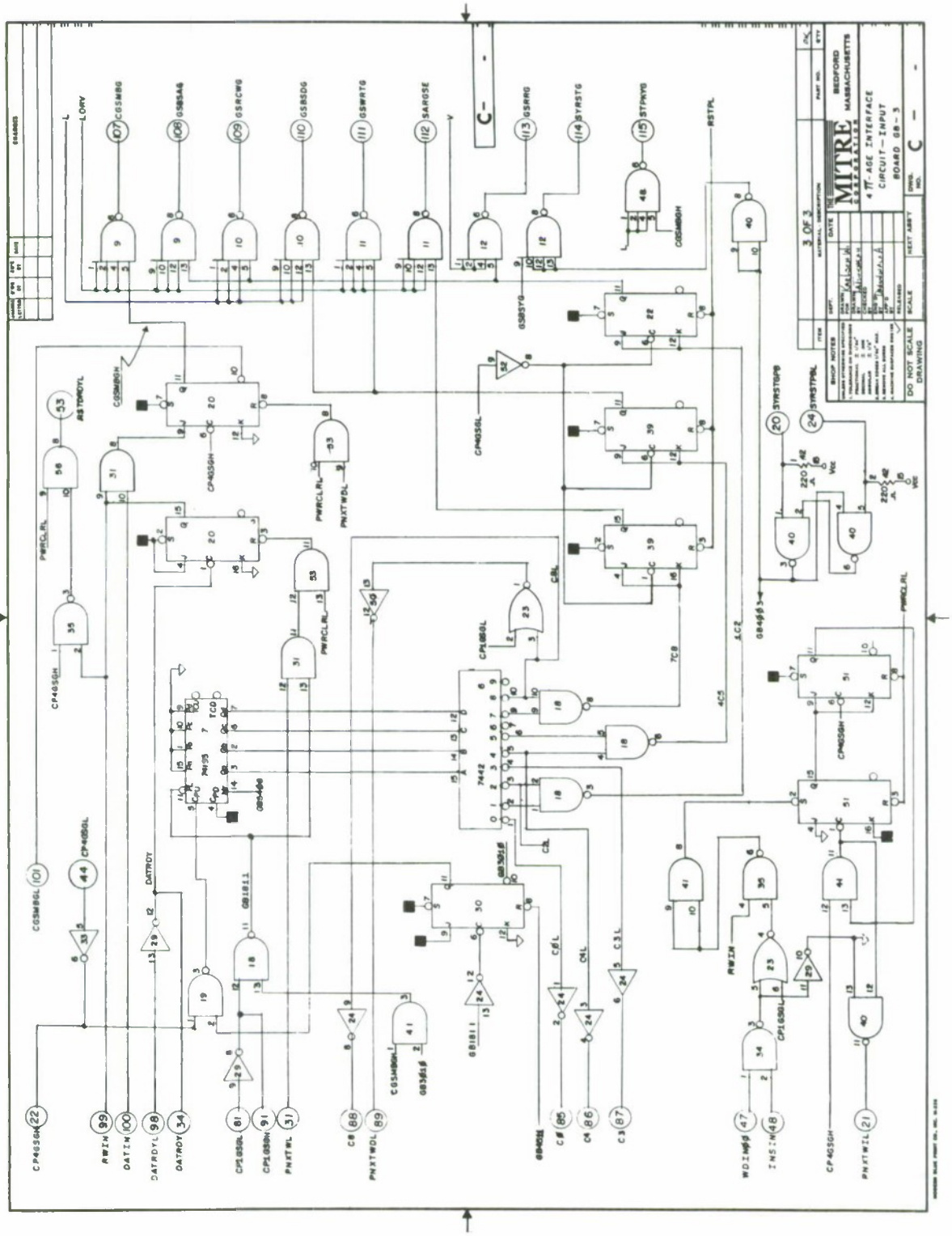


Figure 76 4π-AGE Interface Circuit-Input - Board GB-3

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2. Field Operating Unit (FOU) Operating and Maintenance Manual, International Business Machines, 69-928-43, Owego, New York, January 1970.

3. Operation and Interface Manual Model 250 Digital Cassette Tape Transport, MFE Corporation, Computer Access Systems, Salem, New Hampshire.

4. P.M. Sterpe, Off-Line Cassette Generator Program, Electronic Systems Division/DCN/SALTY NET Program, Technical Paper, Bedford, Massachusetts, 7 September 1976.